Exhibit 12

sought to be filed under seal

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., **Plaintiff,** **v.** **MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC,** **Defendants.**	**Case No. 2:22-cv-203-JRG**

DECLARATION OF NOEL WHITLEY

I, Noel Whitley, declare as follows:

1. I served as Netlist's Vice President of Intellectual Property and Licensing from 2013 to 2019. I have personal knowledge of the facts stated herein, and, if called as a witness, could and would testify to such facts competently under oath.

2. On April 21, 2015, three Micron employees (Dean Klein, Bryan Martin, and Darren Young) visited Netlist's offices in Irvine, California to meet with Netlist. I attended that meeting on behalf of Netlist, as did Christopher Lopes and Rex Sherry. At that meeting, Netlist presented to Micron's employees a presentation titled "Micron/Netlist Partnership Opportunity" (hereafter, the "April 2015 Presentation").

3. I drafted the April 2015 Presentation. I did so with assistance from other Netlist employees at or near the time of the presentation. It was a regular practice for employees of Netlist to communicate with other companies for purposes such as business collaboration opportunities and regarding Netlist's patent portfolio, and to create such presentations to use in meetings with other companies. I understand Netlist preserved a copy of the presentation in the regular course of its business. A true and correct copy of that presentation is attached to this declaration with Bates No. NL-MIC-203_0042085 through -147.

4. At the meeting with Micron on April 21, 2015, Netlist presented every slide in the April 2015 Presentation to Micron's employees.

5. The document with the Bates No. NL-MIC-203_00042083 through -084 is an April 21, 2015 email from Rex Sherry to Chuck Hong, Christopher Lopes, Gail Sasaki, Jay Bhakta, and myself. I received this email at the time it was sent. The email reflects an accurate summary of Netlist's meeting with Micron.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on November 27, 2023.

By: /s/ *Noel Whitley*
Noel Whitley

NETLIST

Micron / Netlist Partnership Opportunity

April 2015

Netlist, Inc. Confidential

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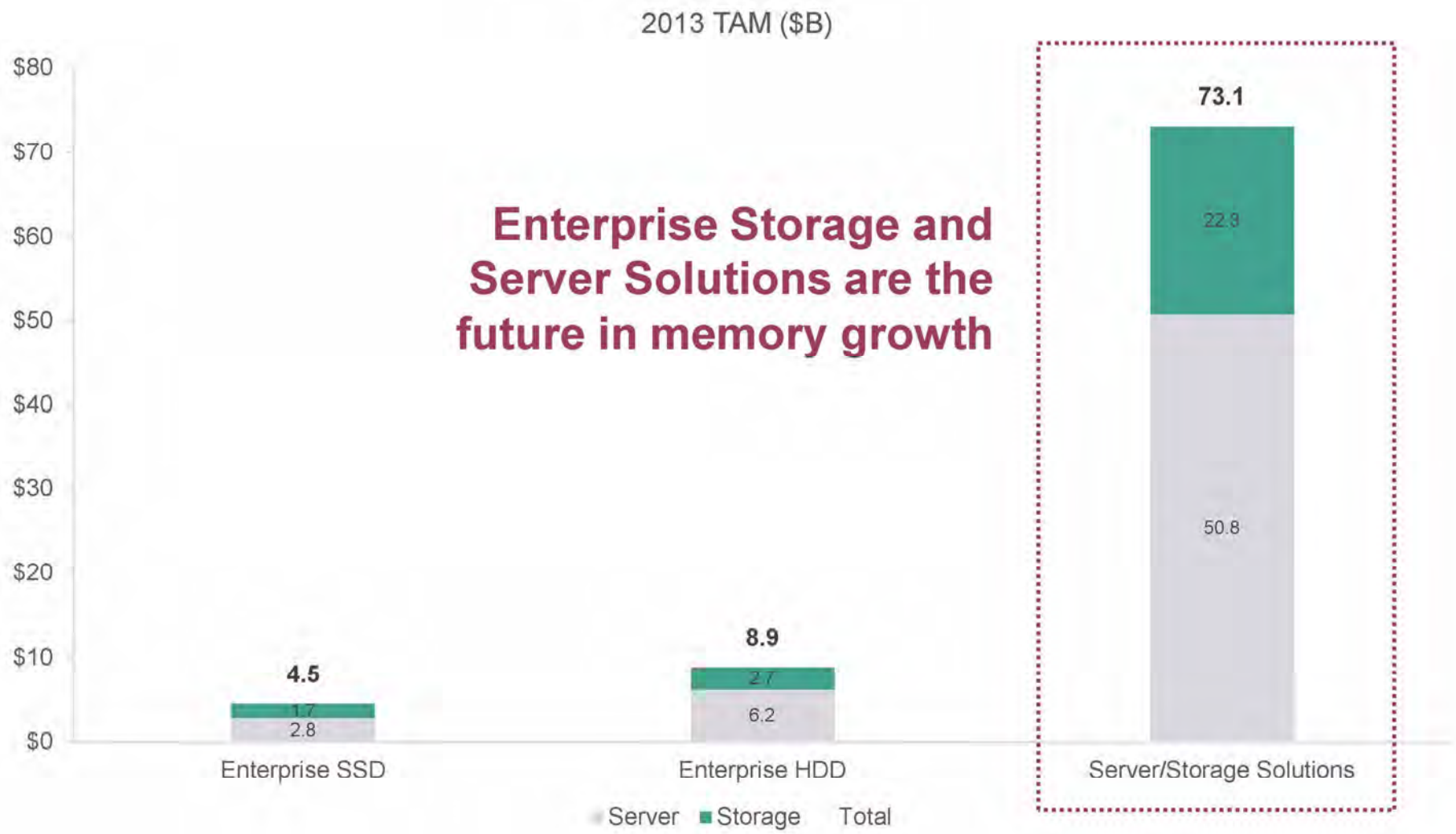
Executive Summary

- **Strategic activity in storage is continuing**
  - Micron/Seagate alliance
- **Major memory players forward integrate into storage for greater margin**

Storage is a Key Market for Memory Companies

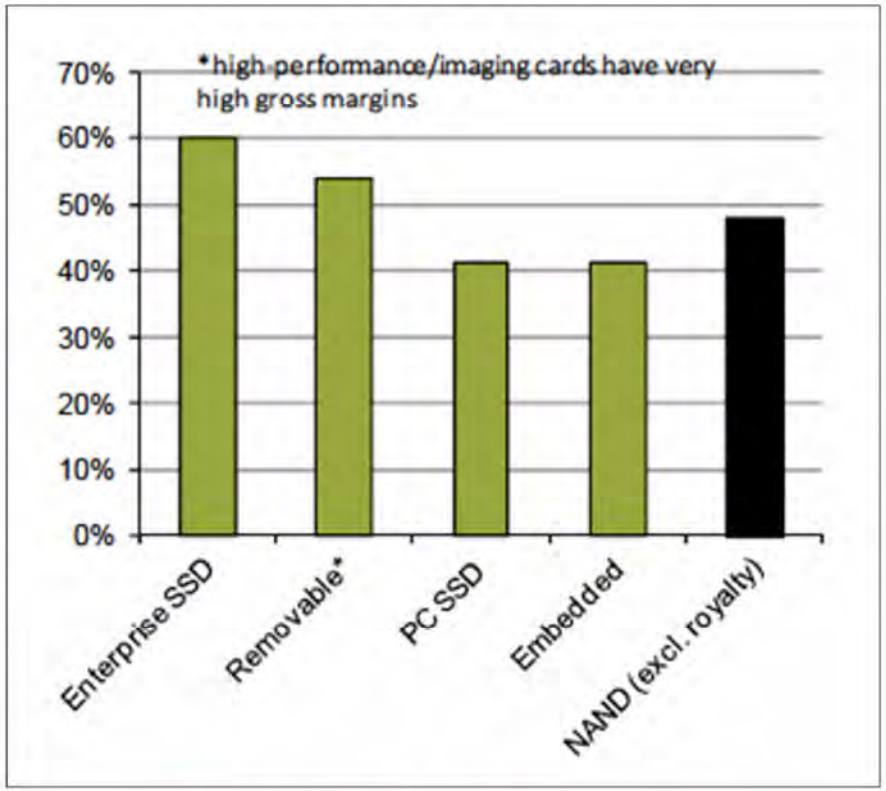
- **Memory channel storage area: heating up, on way to $10B market**
  - SanDisk – ULLtraDIMM shipping
  - Intel
  - HP
  - Microsoft
  - SNIA, ACPI, UEFI
- **Litigation among memory suppliers targeted at big dollars**
  - Rambus/Samsung -- $900 MM
  - SanDisk/Hynix -- $1.1B
  - Toshiba/Hynix -- $ 280M

Future Growth in Memory

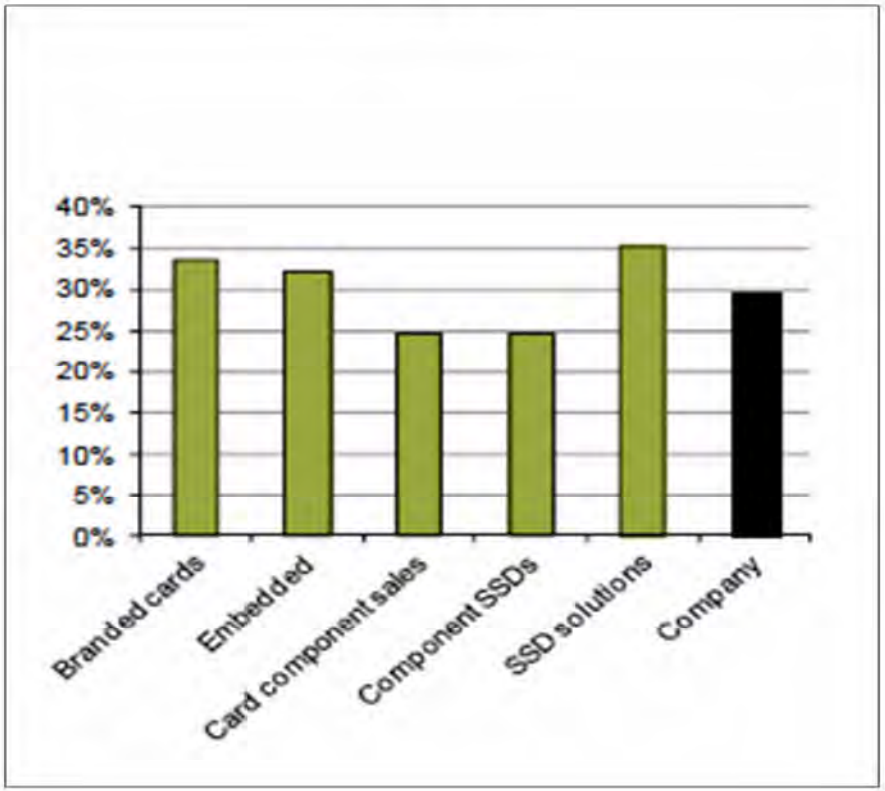


Enterprise Solutions Drives …

SanDisk

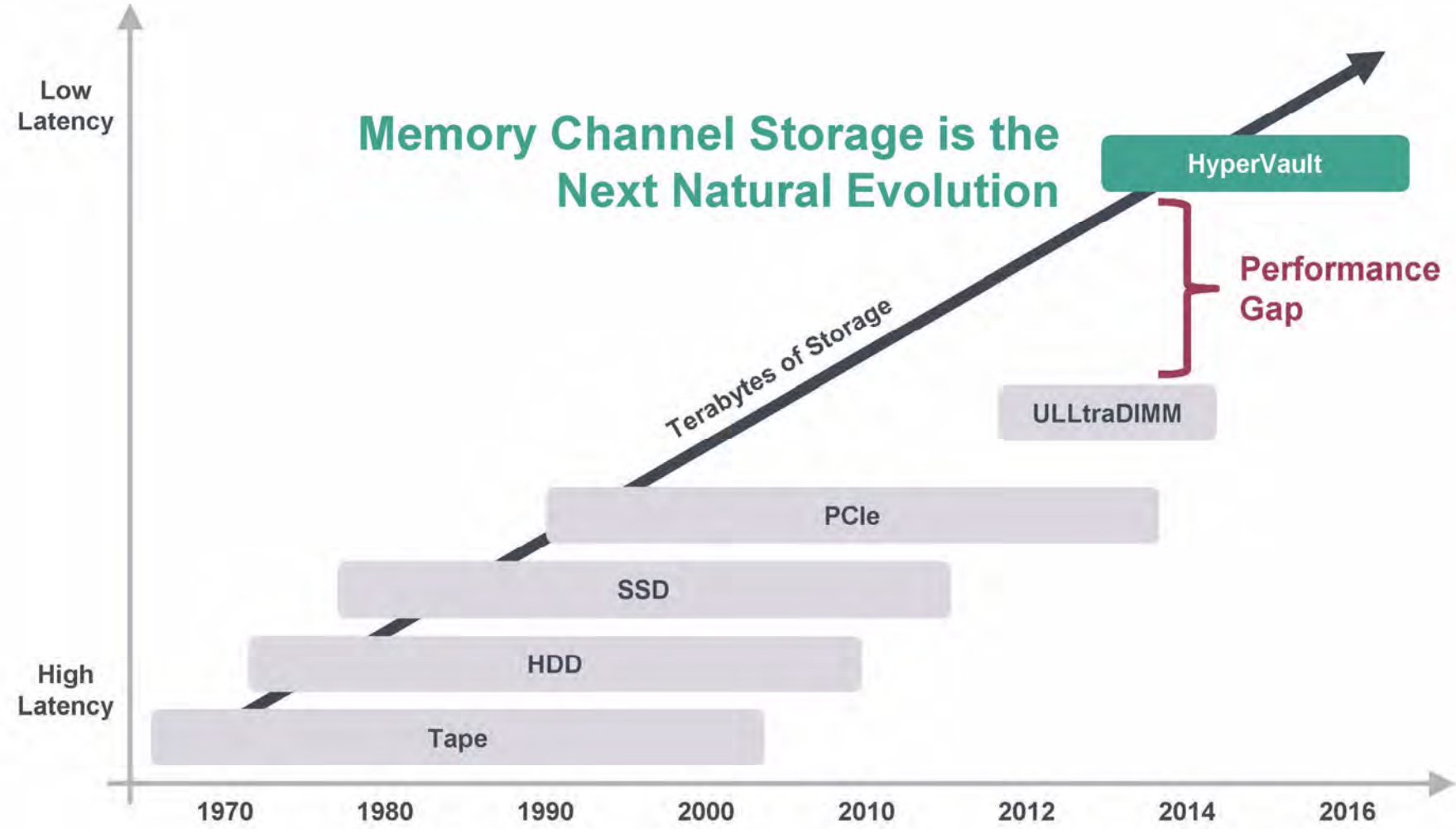


Micron

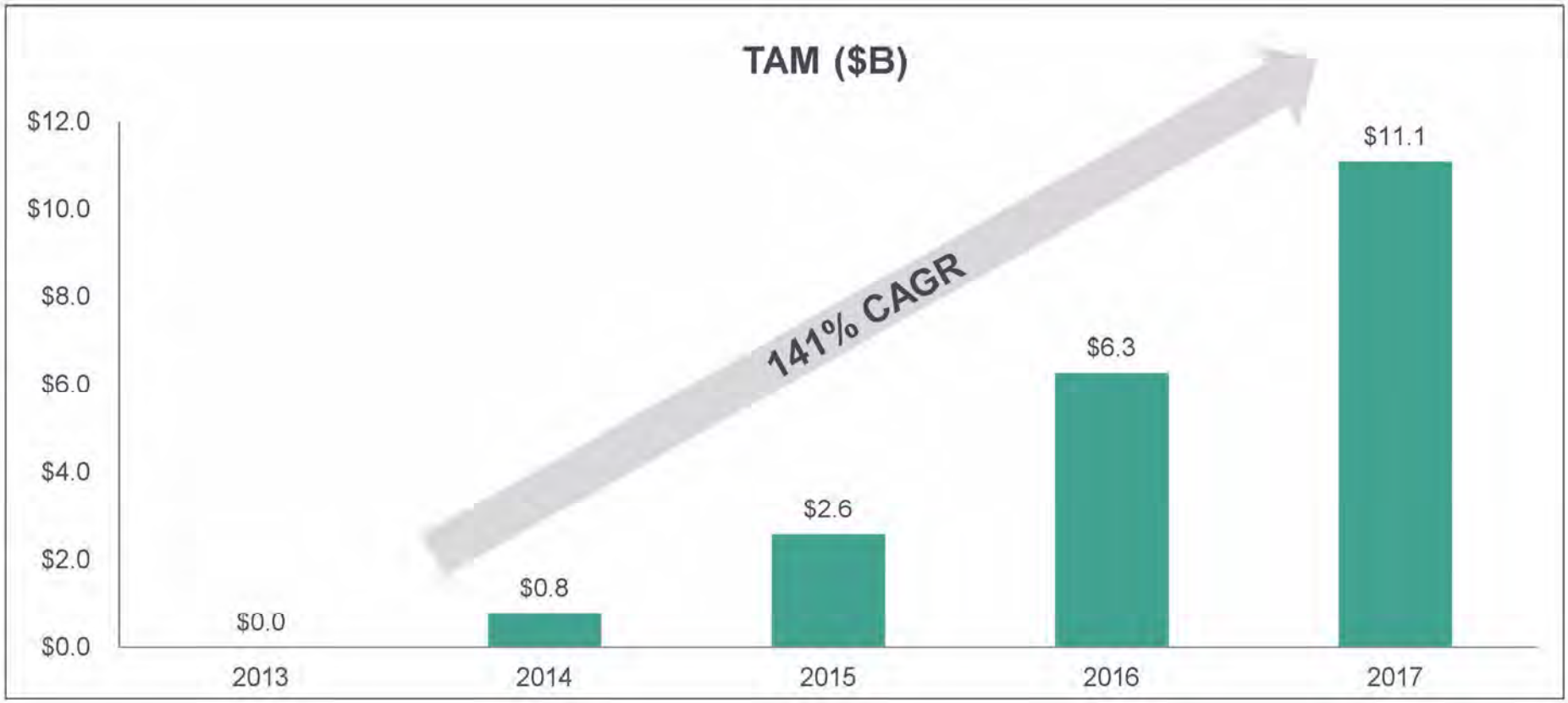


… Higher Margins and Profits

Storage Evolution: the Gap is Widening



Memory Channel SSD Forecast



>$10B Annual Opportunity

Sources: RBC Capital

Storage Landscape – Memory Suppliers

Company	Acquisitions	Alliance/ Partnership	Solutions			LRDIMM	NVDIMM	PCIe	Memory Channel
			DRAM/ Flash	Software/ Firmware	Chipsets				
SanDisk	Pliant; Fusion-io	Diablo	X	X	X	X		X	X
Micron	Virtensys	Agigatech	XX	X	X	X	X		
SK Hynix	Link-a-media Softeq Development Violin Memory		XX	X	X	X	X		
Toshiba	OCZ Technology		X	X	X				
Samsung	Grandis		XX			X			
Kingston	Powerchip	Phison	X		X				

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Business Update

- Partnership with major mobile phone OEM on HyperVault mobile
- Strong new product traction on NVDIMM-N product from major hyperscale companies
- Strengthening Asia and sales teams
- Recently withdrew from JEDEC for NVDIMM
- Strong interest in Netlist IP / product roadmap
- Proceeding along on patent case against SanDisk, Smart Modular and Diablo
- Working on judge ruling on matter of law making preliminary injunction permanent

Netlist Business Model

	HyperVault	IP Licensing	Base Products
Development of next gen. technologies	• Incorporate into new products	• Make available to product partners • Pursue enforcement against those that are not partners	• Incorporate core technologies into existing products
Commercialization Strategies	• Work with partners joint development / marketing	• Leverage partnership deals to enforce against non-partners	• Marketed solely by Netlist
Economics	• 50/50 share with partners	• Upfront payment & running royalties	• 100% to Netlist

Netlist Business Model

Income Statement

Dollars ($ in millions)	Margin
Products	
Core Products	35-40%
Licensing	90%+
HyperVault	>60%
$50-100	**>60%**
Annual Op-ex	30%
Operating Margin	**>30%**

ULLtraDIMM Patent Case

- **Overview**
  - *Patents represent long term value of IP -- Jury verdict has no legal bearing on the patent case*
- **Proceed with Patent Case**
  - Judge granted SanDisk's motion to stay case (Thurs, Apr 9)
  - Drop 4 patents under review to lift the stay
  - Proceed aggressively with remaining 3 patents
- **Strength of Case (3 Patents)**
  - Validity: very strong having survived 2 waves of IPRs
  - Infringement: confirmed solid reads on all 3 patents (8 claims total)
  - Complexity: claims are straight-forward and easily explained to a jury
- **Put DDR4 ULLtraDIMM Product at Risk**
- **Alternative Fee Arrangements**

ULLtraDIMM Trade Secret Case

- **Post-Trial Motions: Reverse jury's finding on breach of contract**
  - Strong on the law: judge can, and should, reverse the Jury's mistake
  - New Trial: we will also argue that a new trial is the appropriate remedy since the mistakes on the contract issue infected the trade secret case as well

- **Post-Trial Motion Process**
  - Motion to dissolve PI is pending while parties brief unfair competition; oral hearing on both issues tentatively set for Friday, Apr 24
  - Reset: we the judge to reset the motion process so that all of these related issues can be briefed and heard together

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Netlist Has One of the Most Valuable Memory IP Portfolios Outside of the Big 4 and the Major NPEs

- **>10 years invested in Building IP Portfolio**
- **$60 MM invested in building seminal IP related to LRDIMMs and Hybrid Memory**
- **Withdrawing from NVDIMM standardization efforts at JEDEC**
- **Patent portfolio has fundamental patents that are battle tested and have become increasingly valuable**
  - Seminal distributed buffer architecture patent survived 2 IPR petitions
  - Another seminal patent on Load Reduction and Rank Multiplication survived a multi-year Reexam
  - Two seminal hybrid memory patents each survived 2 IPR petitions
  - 3rd party validation rankings validate value of portfolio

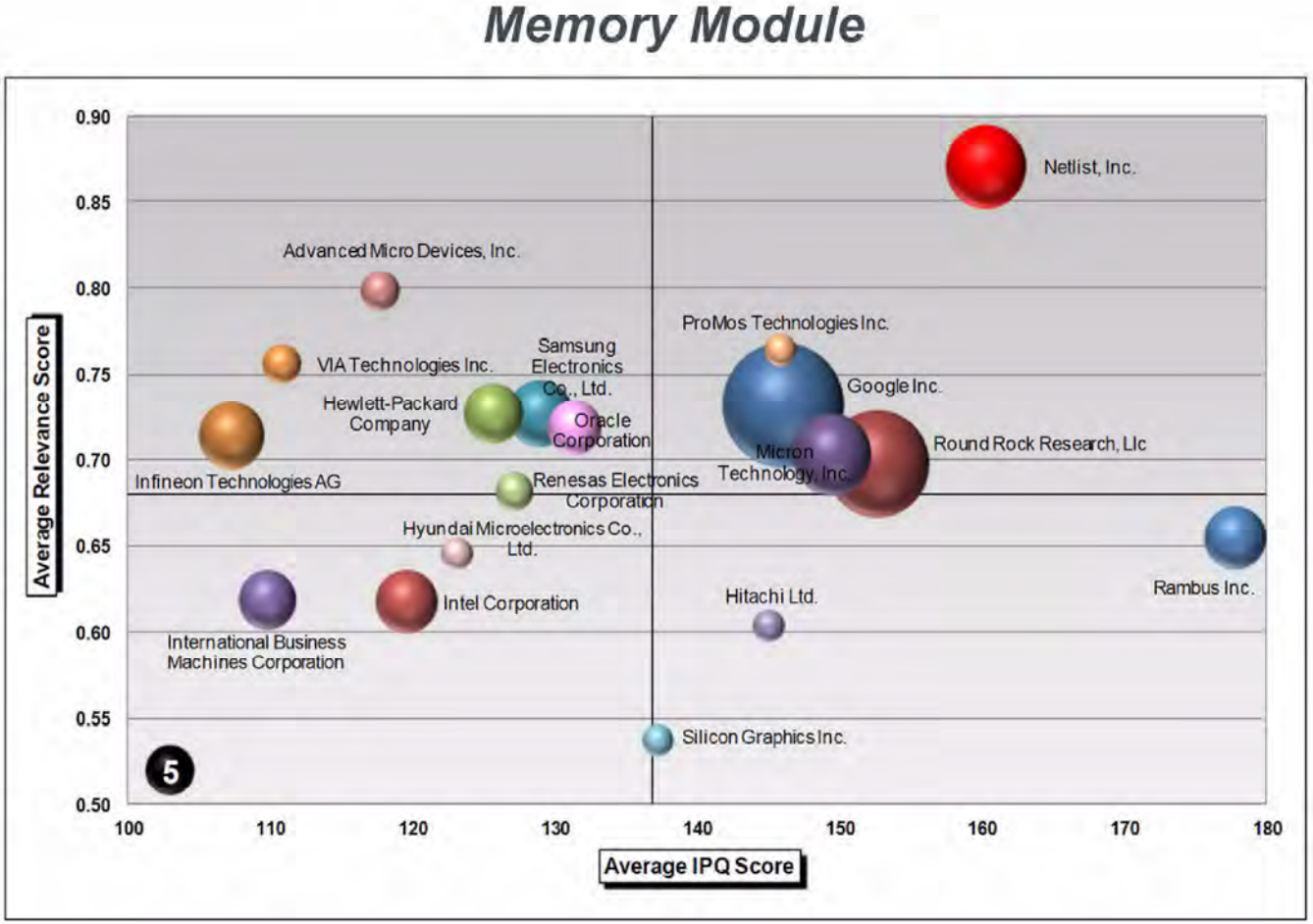
Netlist IP Litigation

- **History of aggressively protecting Netlist IP**
- **Google and Inphi cases are stayed pending reexaminations**
- **Seminal '537 patent already emerged, others to follow**

Netlist Patent	Asserted Against	Suit Filed (Year)
7,298,386	Google	2009
7,619,912	Google, Inphi	2009
7,532,537	**Inphi**	**2009**
7,636,274	Inphi	2009
7,881,150	SanDisk, Diablo	2013
8,081,536	SanDisk, Diablo	2013
8,001,434	SanDisk, Diablo	2013
8,359,501	SanDisk, Diablo	2013
8,516,185	**SanDisk, Diablo**	**2013**
8,301,833	**SanDisk, Diablo**	**2013**
8,516,187	**SanDisk, Diablo**	**2013**
Bold Patents = Survived re-exam at USPTO		

- **Netlist's Position vis-à-vis LRDIMM**
  - Validity: 2 Untouchable patents that survived reexamination in PTO
  - Infringement: Clearly documented vs. standard (SEPs)

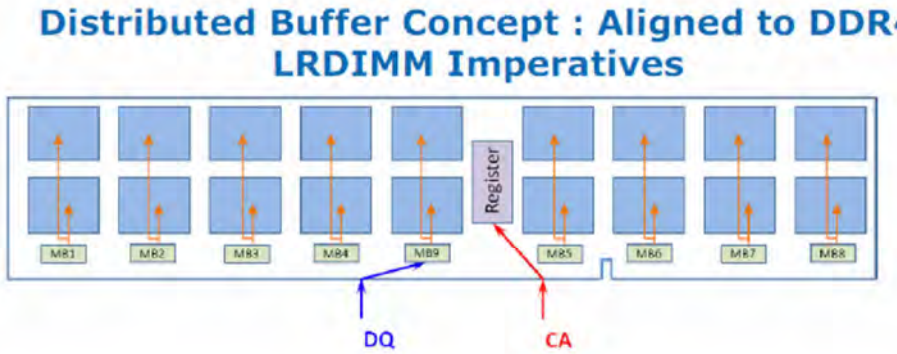
Ocean Tomo Patent Rating



Netlist: Fundamental IP in DIMMs

Netlist's seminal patent covering the distributed buffer architecture is unavoidable and THE fundamental patent in LRDIMM and Hybrid memory

- DDR4 distributed buffer architecture adopted by JEDEC is a copy of Netlist's HCDIMM topology



- Netlist's distributed buffer architecture is a seminal patent (8,516,185)
  - Survived 2 IPRs from SanDisk and reads on DDR3 and DDR4 LRDIMM and memory channel storage products

Portfolio Comparison: Netlist v. Diablo

LRDIMM / Memory Channel

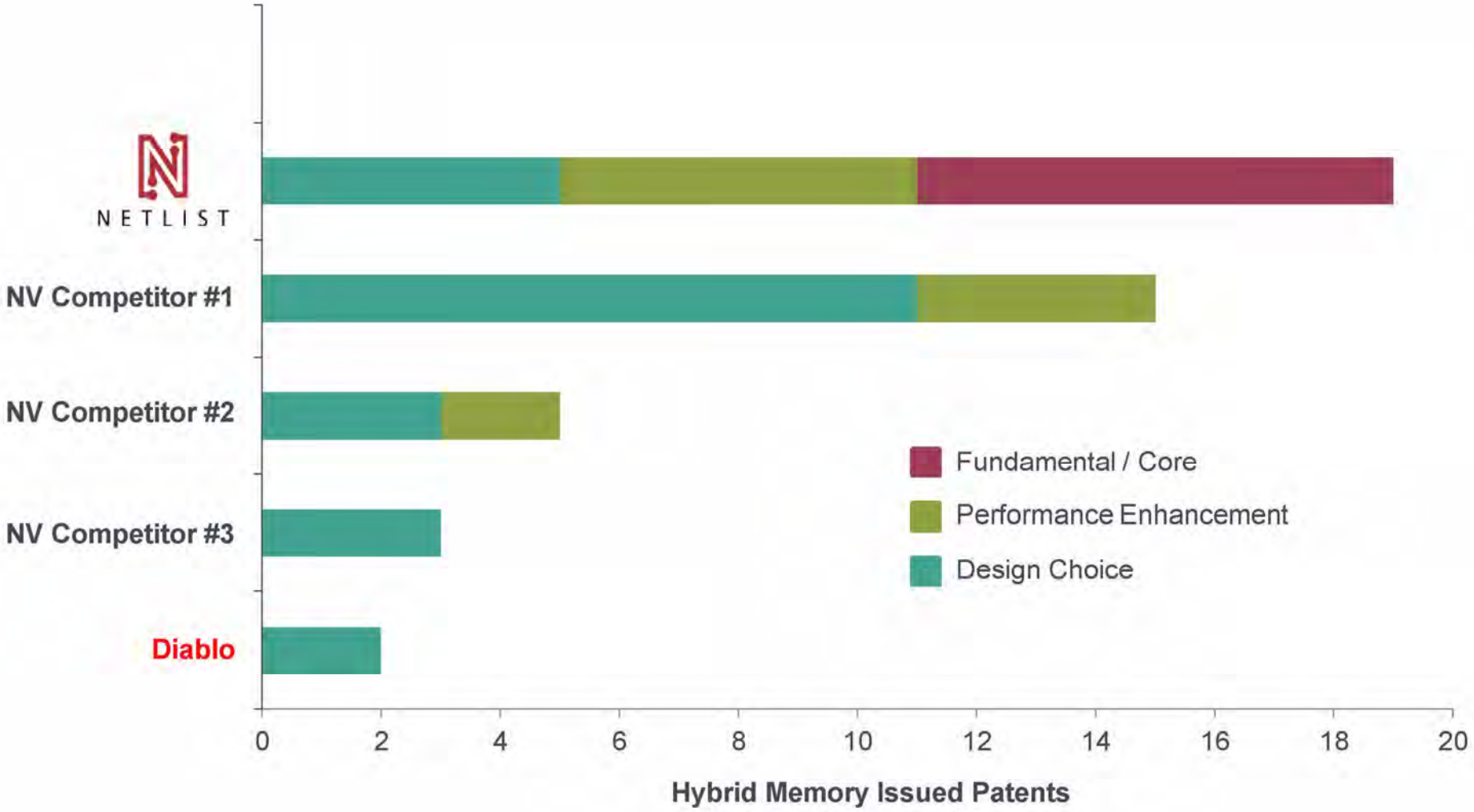
	Patents	Earliest Priority	Patents Asserted	Survived Reexam/IPR	Seminal or High Value
Netlist	43	2004	8	2	7
Diablo	3*	2008	0	0	0

*Netlist is licensed to these Diablo patents

Hybrid Memory

	Patents	Earliest Priority	Patents Asserted	Survived Reexam/IPR	Seminal or High Value
Netlist	8	2007	3	2	6
Diablo	2	2011	0	0	0

Hybrid Memory Portfolio Comparison



Patent Portfolio Highlights

Largest Collection of Battle Tested LRDIMM, NVMe, Hybrid Memory and Memory Channel Storage Patents

Classification	LRDIMM	Alpha Score*	Hybrid	Alpha Score*
SEMINAL	7,532,537 (Load Reduction, Rank Multiplication)	90	8,301,833 (Clock Throttling)	86
	8,516,185 (Distributed Buffer Architecture)	92	8,516,187 (Data Segmentation)	82
HIGH VALUE	8,417,870	90	8,671,243	83
	8,756,364	87	8,874,831	73
	8,516,188	84	8,904,099	NR
	7,619,912	84	8,880,791	NR
	7,636,274	81		
PROMISING	7,916,574	80		
	7,864,627	77	8,677,060	NR
	7,881,150	76	8,904,098	NR
	8,081,536	70		

*Patents rated by OPus on a 100-Point Scale (Alpha Score):

90+	Rare
75+	Compelling

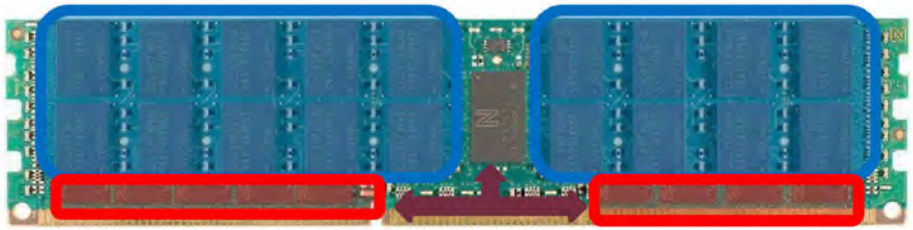
Seminal LRDIMM Patent: 7,532,537

U.S. Pat. No.	7,532,537
Filing Date	Jan 19, 2006
Earliest Priority	Mar 5, 2004
Issue Date	May 12, 2009
Alpha Score	RARE (90.12)

- Survived multi-year Reexam from Inphi (on appeal at CAFC)
- Covers DDR3 & DDR4 LRDIMM
- Asserted against Inphi

Claims Generally Require a DIMM with:

- DDR DRAM
- **Buffers**
- Load Reduction
- Rank Multiplication (using chip select signals)



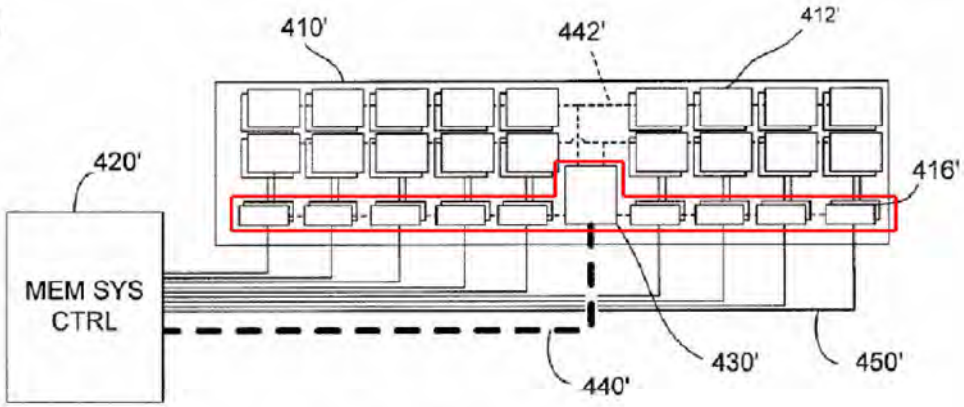
Seminal LRDIMM Patent: 8,516,185

U.S. Pat. No.	8,516,185
Filing Date	April 15, 2010
Earliest Priority	July 16, 2009
Issue Date	Aug 20, 2013
Alpha Score	RARE (91.68)

- Survived Two IPR Requests from SanDisk and Smart Modular
- Covers DDR3 & DDR4 LRDIMM
- Asserted against ULLtraDIMM

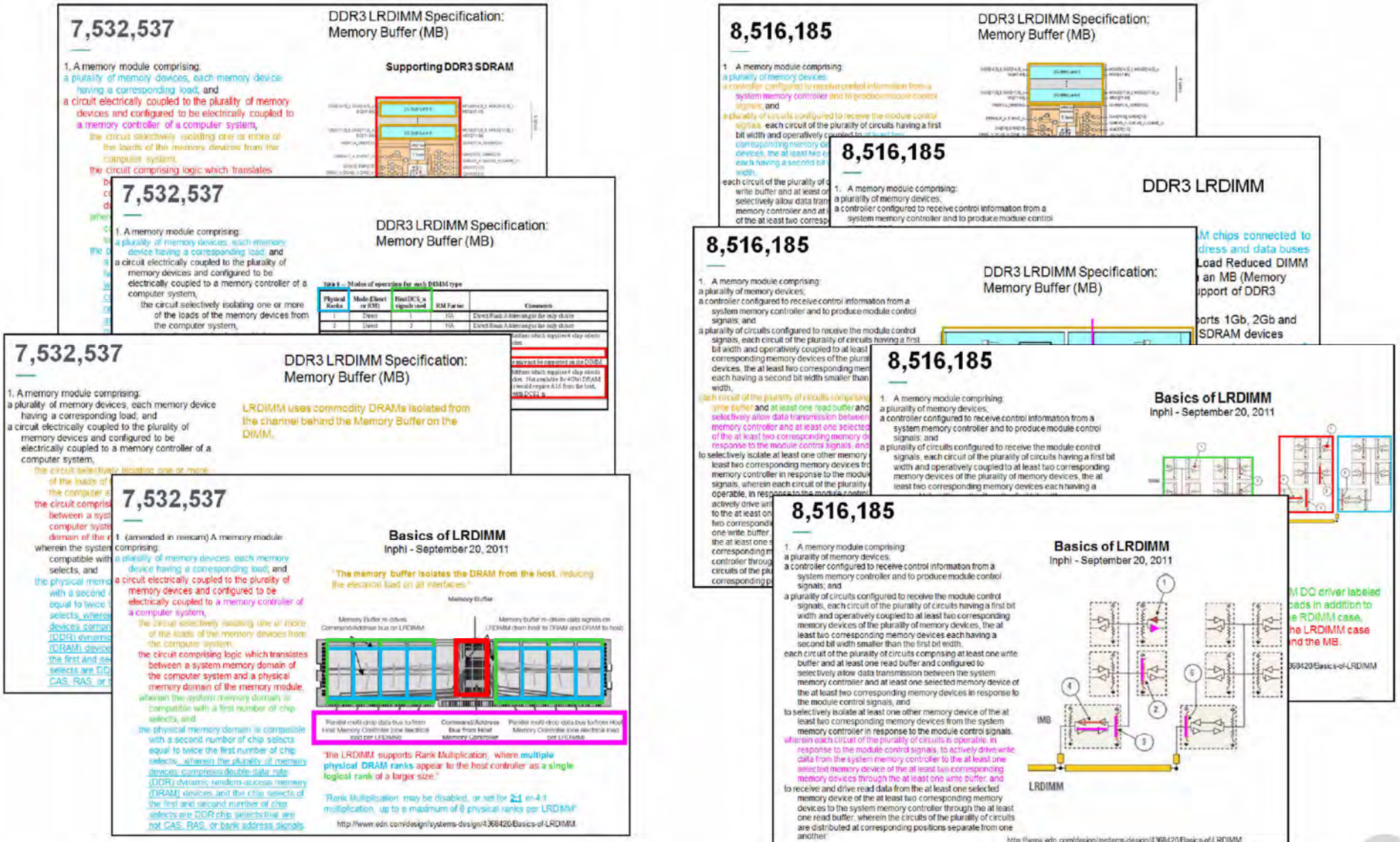
Claims Generally Require a DIMM with:

- Buffered Groups of Memory Devices (e.g., DRAM, Flash)
- Control Circuit
- Load Reduction



'185 FIG. 3C

Documented Coverage of LRDIMM DDR3 & DDR4

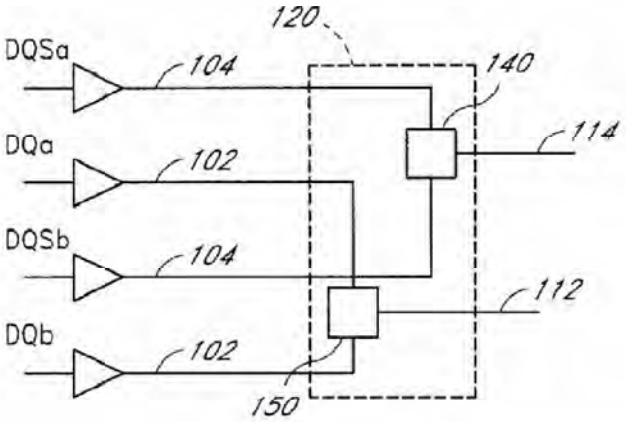


LR in Memory Package: 8,756,364

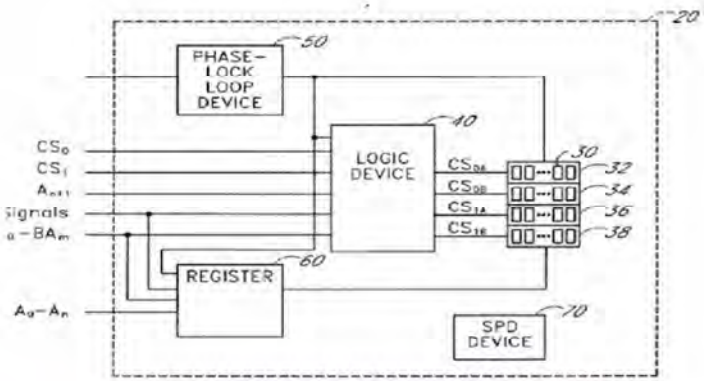
U.S. Pat. No.	8,756,364
Filing Date	November 1, 2011
Earliest Priority	March 5, 2004
Issue Date	June 17, 2014
Alpha Score	Compelling (87.16)

Multi-Rank Memory Module with Load Reduction:

- Memory Devices in Ranks
- Logic to enable data communication with load reduction
- Enabling based on latency values



'364 FIG. 6D



'364 FIG. 1A

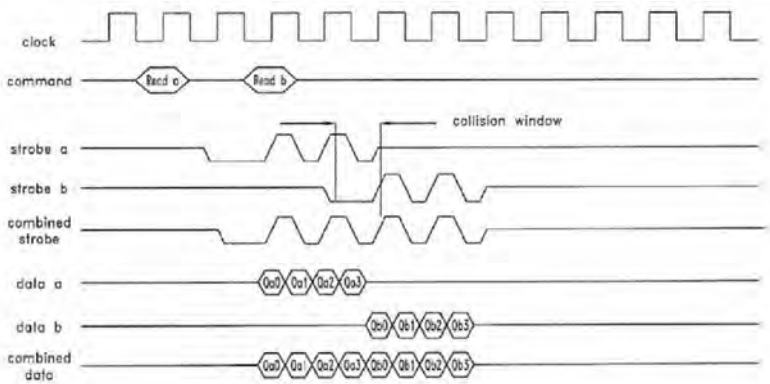
- Covers load reduction implemented on the module or within the memory package

LR in Memory Package: 8,516,188

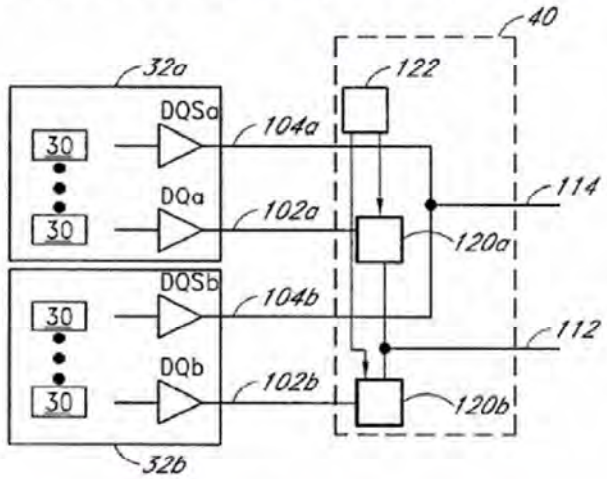
U.S. Pat. No.	8,516,188
Filing Date	November 1, 2011
Earliest Priority	March 5, 2004
Issue Date	August 20, 2013
Alpha Score	Compelling (84.46)

A Load Reduction Circuit:

- Selective coupling of two sets of DQ and DQS lines to data bus
- Data signal merging in response to multiple commands
- Supports Frequency multiplication



'188 FIG. 7



'188 FIG. 5C

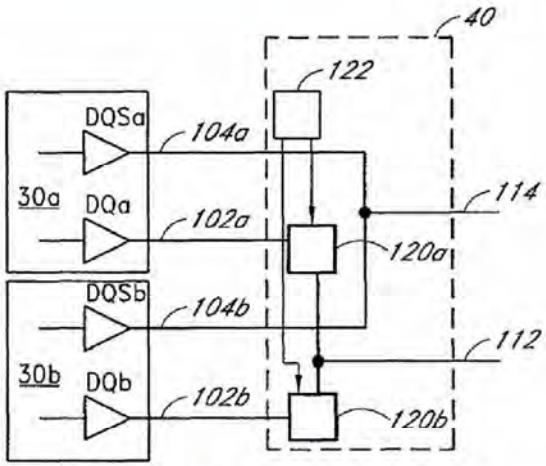
- Covers load reduction implemented on the module or within the memory package

LR in Memory Package: 13/971,231

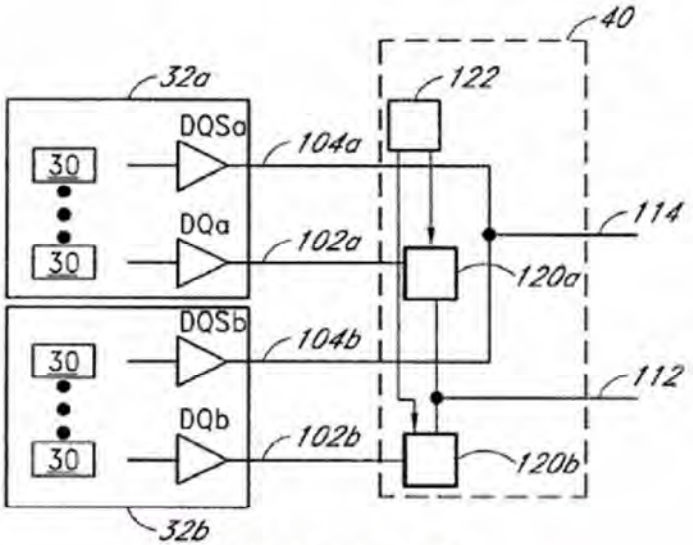
U.S. Pat. No.	13/971,231
Filing Date	August 20, 2013
Earliest Priority	March 5, 2004
Issue Date	To be issued May 2015
Alpha Score	N/A

Load Reduction:

- Selective coupling of two memory devices to the memory bus according to memory commands
- Allows data interleaving



'231 FIG. 5A



'231 FIG. 5C

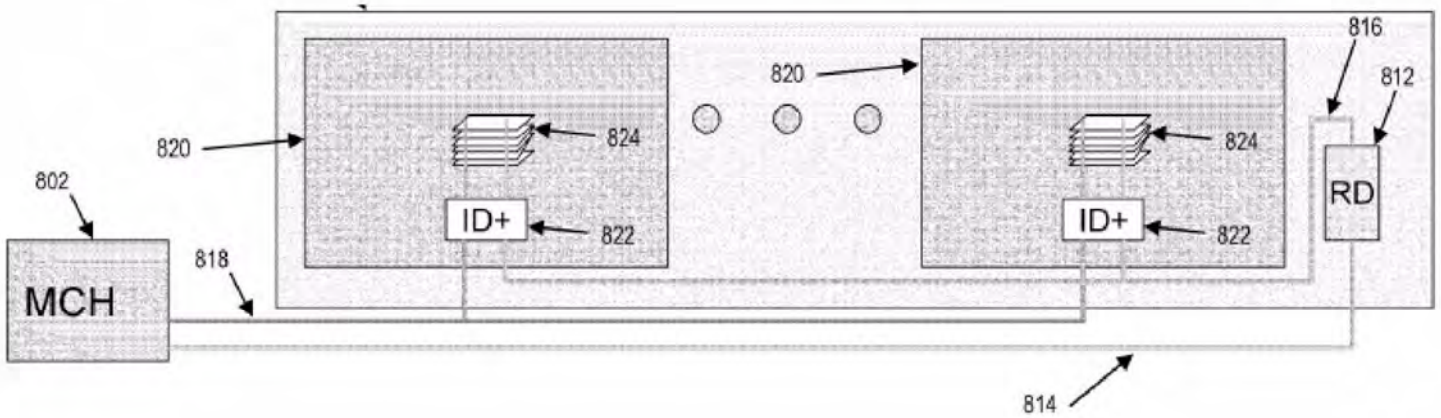
- Covers load reduction implemented on the module or within the memory package

TSV: 8,787,060

U.S. Pat. No.	8,787,060
Filing Date	November 3, 2011
Earliest Priority	November 2, 2010
Issue Date	July 22, 2014
Alpha Score	Promising (69.87)

Claims Load Reduction TSV Packages and memory module having:

- Buffered DRAM Stacks with Load Reduction
- Enhanced Register
- Control Die with Driver Optimization
- Grouping the DRAM dies for noise reduction



'060 FIG. 8

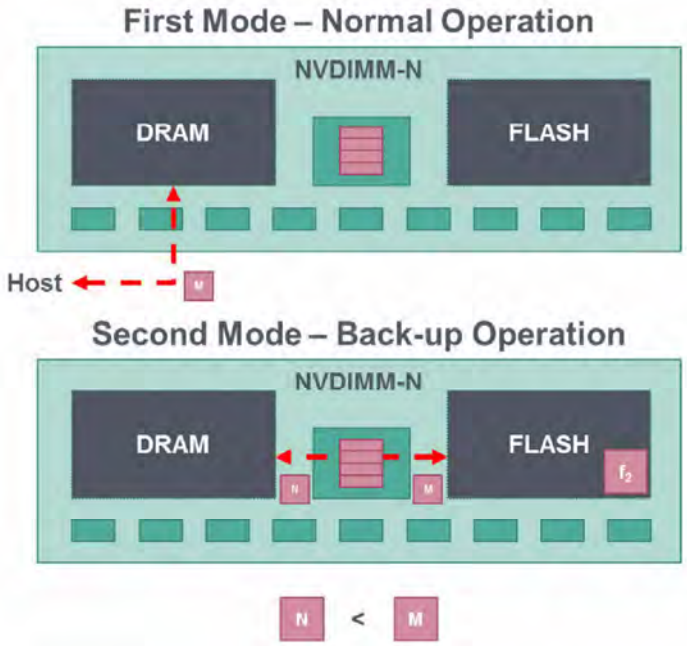
Seminal Hybrid Patent: 8,516,187

U.S. Pat. No.	8,516,187
Filing Date	June 28, 2012
Earliest Priority	June 1, 2007
Issue Date	Aug 20, 2013
Alpha Score	Compelling (81.85)

- Survived Two IPR Requests from SanDisk and Smart Modular
- Asserted against ULLtraDIMM

Claims Generally Require a DIMM with:

- DRAM and FLASH
- First Mode: DRAM communicates full data words to/from Host
- Second Mode: DRAM transfers data to FLASH via a buffer in segments smaller than a full data word



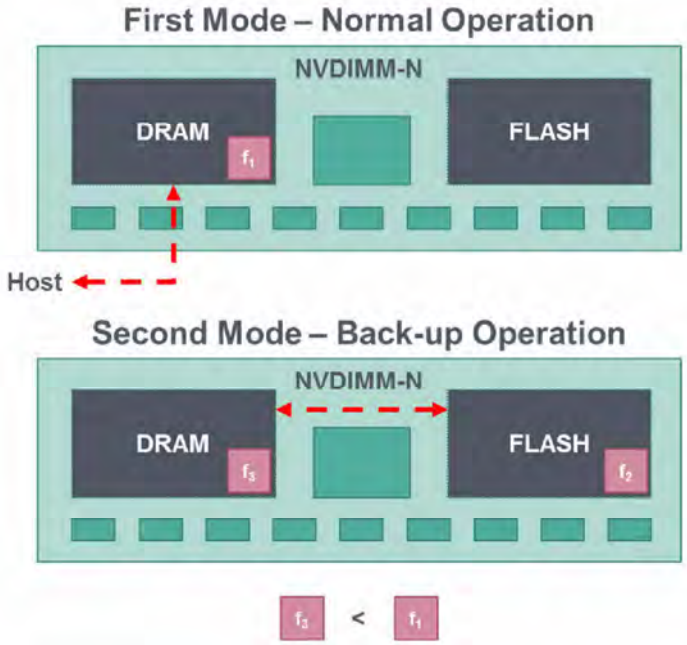
Seminal Hybrid Patent: 8,301,833

U.S. Pat. No.	8,301,833
Filing Date	Sep 29, 2008
Earliest Priority	June 1, 2007
Issue Date	Oct 30, 2012
Alpha Score	Compelling (86.03)

- Survived Two IPR Requests from SanDisk and Smart Modular
- Asserted against ULLtraDIMM

Claims Generally Require a DIMM with:

- DRAM and FLASH
- First Mode: DRAM operates at a first frequency during normal operation
- Second Mode: DRAM operates at a second, lower frequency during data transfers to/from FLASH



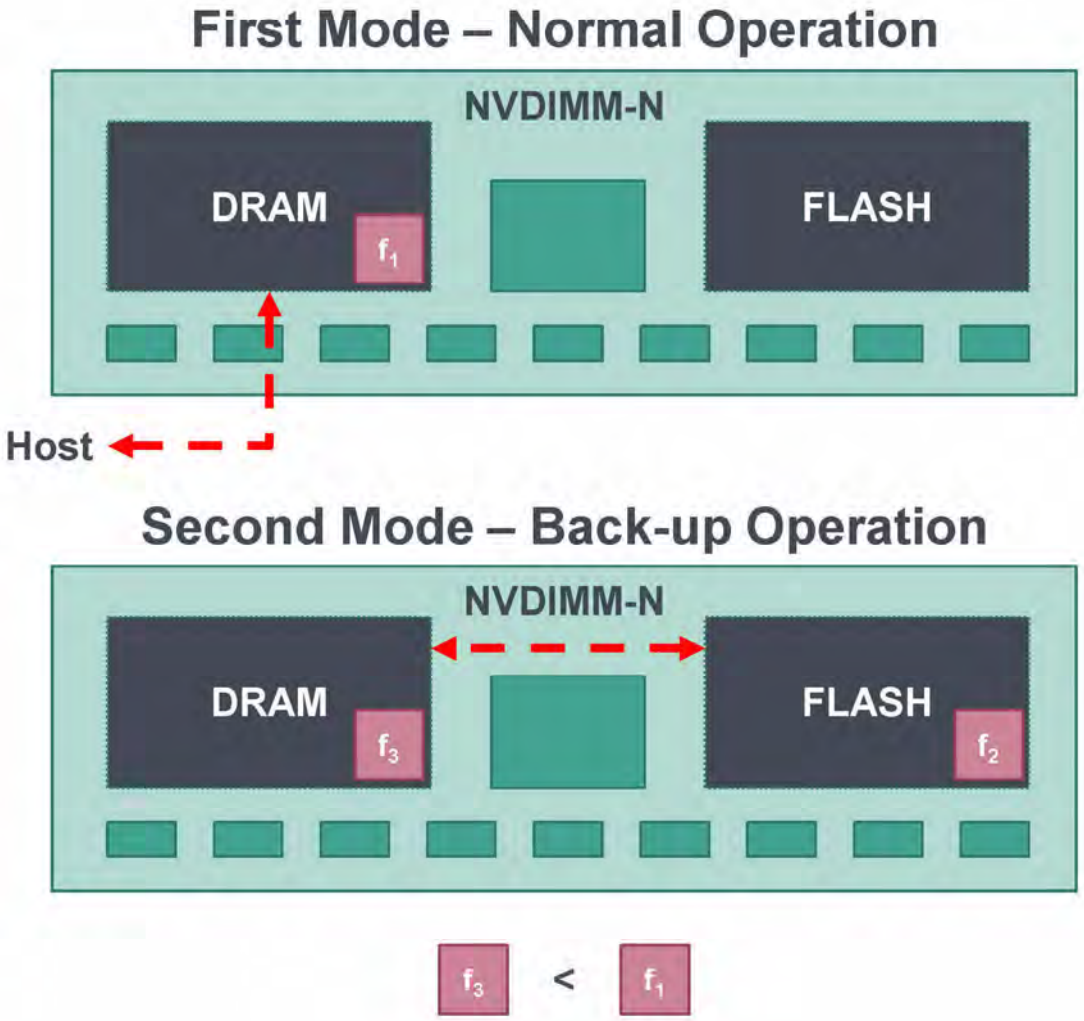
Example Hybrid Claim Analysis: 8,301,833

1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

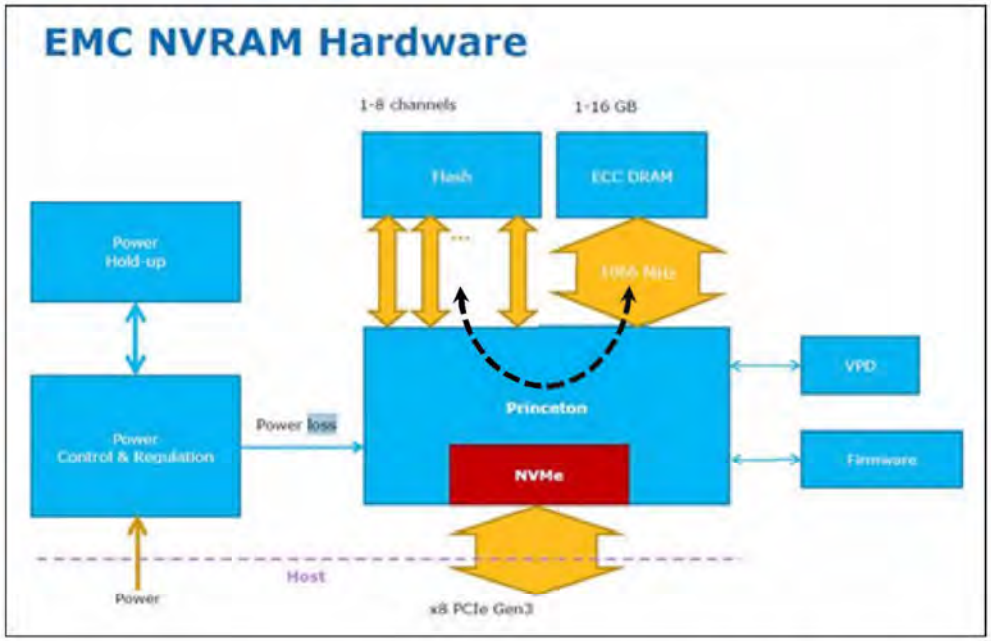
operating the volatile memory subsystem at a first clock frequency when the memory system is in a **first mode** of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a **second mode** of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the **third clock frequency being less than the first clock frequency**.



NVMe: 8,301,833



Claims Generally Require a DIMM with:

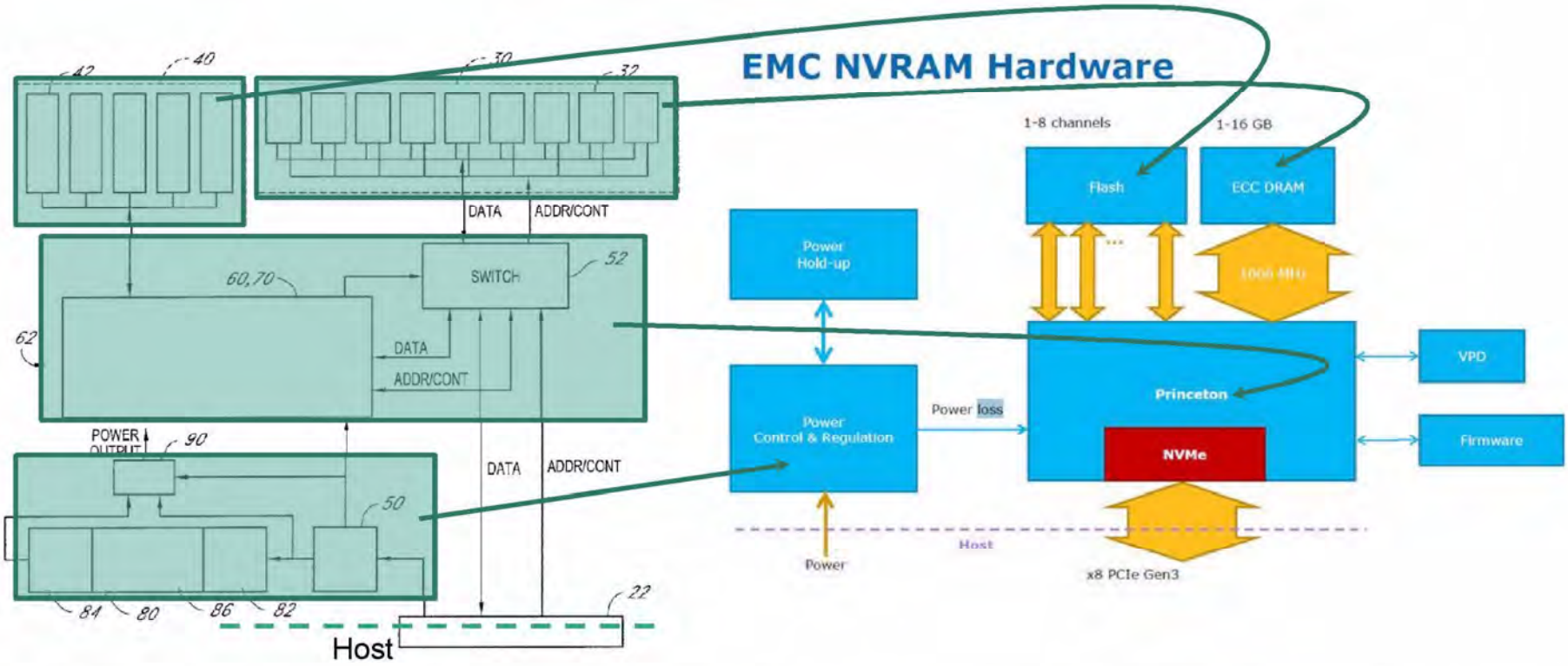
- Volatile and Non-Volatile memory
- First Mode: Volatile operates at a first frequency during normal operation
- Second Mode: Volatile operates at a second, lower frequency while data is transferred to/from Non-Volatile memory

DDR4 Standard enables operating Volatile memory at a second, lower frequency:

"2.1.4 Dual Frequency Support
The DDR4DB01 supports operation at a second, i.e. ***lower than nominal, frequency*** *as a means to save RCD/DB and* ***DRAM*** *power when the memory bandwidth demand allows."*
Source: DDR4 Data Buffer, July 2013, p.8

"2.8 Dual Frequency Support
The DDR4 register supports operation at a second, i.e. ***lower than nominal, frequency*** *as a means to save buffer and* ***DRAM*** *power when the memory bandwidth demand allows."*
Source: DDR4 Register, July 2013, p.35

NVMe: Hybrid Memory Patent Family



Architecture mapping of Netlist Hybrid Memory to NVMe architecture as illustrated by block diagram of EMC's first use of NVMe standard.

Source: NVM Express: Optimized Interface for PCI Express, Intel IDF13, pp-50-51

Earliest Patent Priority in Industry (2007)

Patent Portfolio Summary

Category	Technology	US Issued	US Pending	Foreign Granted	Foreign Pending
LRDIMM	Rank multiplication & load reduction	14	1		
	Distributed buffer architecture	2	1	2	6
Hybrid Memory	Architectures	6	6		3
	Key Features	2	7		
Performance	DDR performance		2		
	Interoperability		1		
	Handshaking	1	1		
	Load isolation in 3DS	1	1		
	Mode refresh	2			
	Module self-test	3	1		
	Load isolation noise reduction	2	1		
High Density	High density modules	4			
	Stacked substrates	5	1		
	High density with Flex	4	1		
	High density 3R		1		
Thermal	Heat spreader in high density modules	3			
	Heat dissipation in high density modules	2			

LRDIMM Portfolio

Alpha Score	Title	US Pat No.	In Suit?	Reexam or IPR	Ref. Count	Fwd. Cites	Highlights
91.68	System and method utilizing distributed byte-wise buffers on a memory module	8,516,185	Y	Y	296	4	- *Survived two IPR petitions from SanDisk and Smart Modular with NO claims reviewed* - Covers fundamental distributed buffer architecture used at DDR3 & DDR4 - Asserted against ULLtraDIMM
90.4	System and method of increasing addressable memory space on a memory board	8,417,870			296	2	- Parent patent of '185
90.12	Memory module with a circuit providing load isolation and memory domain translation	7,532,537	Y	Y	66	86	- *Survived multi-year Reexamination with all 60 claims confirmed by PTAB; on appeal at CAFC* - Fundamental DDR3 and DDR4 LRDIMM
87.16	Multirank DDR memory module with load reduction	8,756,364			491	1	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered
84.46	Circuit for memory module	8,516,188			417	2	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered
84.34	Memory module decoder	7,619,912	Y	Y	236	75	- Faring well in multi-year Reexamination with 90+ claims allowed by examiner - Currently on appeal at PTAB
81.14	Memory module with a circuit providing load isolation and memory domain translation	7,636,274	Y	Y	236	23	- In Reexamination pursuing claims covering DDR3 and DDR4 LRDIMM
80.89	High-density memory module utilizing low-density memory components	7,286,436			28	77	- Earliest patent in LR/RM family
80.04	Circuit providing load isolation and memory domain translation for memory module	7,916,574			291	7	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered
77.28	Memory module decoder	7,289,386	Y	Y	41	88	- Asserted against Google - Broad claims in multi-year Reexamination
76.9	Memory module decoder	7,864,627		Y	284	16	- Broad claims in multi-year Reexamination
75.73	Circuit providing load isolation and memory domain translation for memory module	7,881,150	Y		284	16	- Asserted against ULLtraDIMM - Currently under IPR review
70.19	Circuit for memory module	8,081,536	Y		318	3	- Asserted against ULLtraDIMM - Currently under IPR review
65.93	Circuit for providing chip-select signals to a plurality of ranks of a DDR memory module	8,081,535			321	2	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered
64.94	Circuit for providing chip-select signals to a plurality of ranks of a DDR memory module	8,081,537			315	2	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered
63.48	Circuit providing load isolation and memory domain translation for memory module	8,072,837			312	2	- Fundamental DDR3 and DDR4 LRDIMM - All reexamination art considered

Hybrid Memory Portfolio

Alpha Score	Title	US Pat No.	In Suit?	Reexamor IPR	Ref. Count	Fwd. Cites	Highlights
86.03	Non-volatile memory module	8,301,833	Y	Y	14	10	- *Survived two IPR petitions from SanDisk and Smart Modular with NO claims reviewed* - Covers fundamental architectural elements of hybrid memory DIMMs - Asserted against ULLtraDIMM
83.3	Isolation switching for backup memory	8,671,243			40	5	- Covers fundamental architectural elements of hybrid memory DIMMs
81.85	Data transfer scheme for non-volatile memory module	8,516,187	Y	Y	23	7	- *Survived two IPR petitions from SanDisk and Smart Modular with NO claims reviewed* - Covers fundamental architectural elements of hybrid memory DIMMs - Asserted against ULLtraDIMM
73.09	Flash-DRAM hybrid memory module	8,874,831				0	- Covers fundamental architectural elements of hybrid memory DIMMs, particularly NVDIMM-P
*	Isolation switching for backup of registered memory	8,677,060			*	*	- Covers fundamental architectural elements of hybrid memory DIMMs
*	Isolation switching for backup memory	8,904,099			*	*	- Covers fundamental architectural elements of hybrid memory DIMMs
*	Isolation switching for backup of registered memory	8,880,791			*	*	- Covers fundamental architectural elements of hybrid memory DIMMs
*	Redundant backup using non-volatile memory	8,904,098			*	*	- Covers fundamental architectural elements of hybrid memory DIMMs

*Patent not yet analyzed

DIMM Technologies Portfolio

Alpha Score	Title	US Pat No.	In Suit?	Reexam or IPR	Ref. Count	Fwd. Cites	Highlights
90.07	Systems and methods for refreshing a memory module	8264903			2	5	
88.98	Arrangement of integrated circuits in a memory module	6751113			42	163	
86.9	High density memory module using stacked printed circuit boards	7254036			26	70	
84.87	Circuit providing load isolation and noise reduction	8782350			308	1	
83.35	Memory board with self-testing capability	8001434	Y	Y	85	10	- Asserted against ULLtraDIMM - Under IPR review
82.64	Memory board with self-testing capability	8359501	Y	Y	89	3	- Asserted against ULLtraDIMM - Under IPR review
82.53	Heat dissipation for electronic modules	8705239			183	2	
79.54	Memory module having thermal conduits	8488325			138	2	
73.05	Module having at least two surfaces and at least one thermally conductive layer therebetween	8345427			138	1	
71.76	High density module having at least two substrates and at least one thermally conductive layer therebetween	7630202			131	12	
70.54	Electronic module with flexible portion	8864500			148	0	

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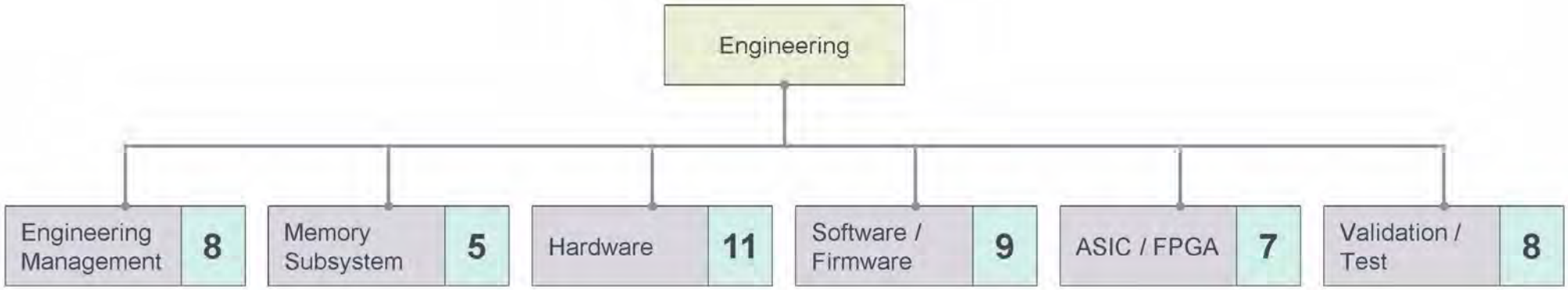
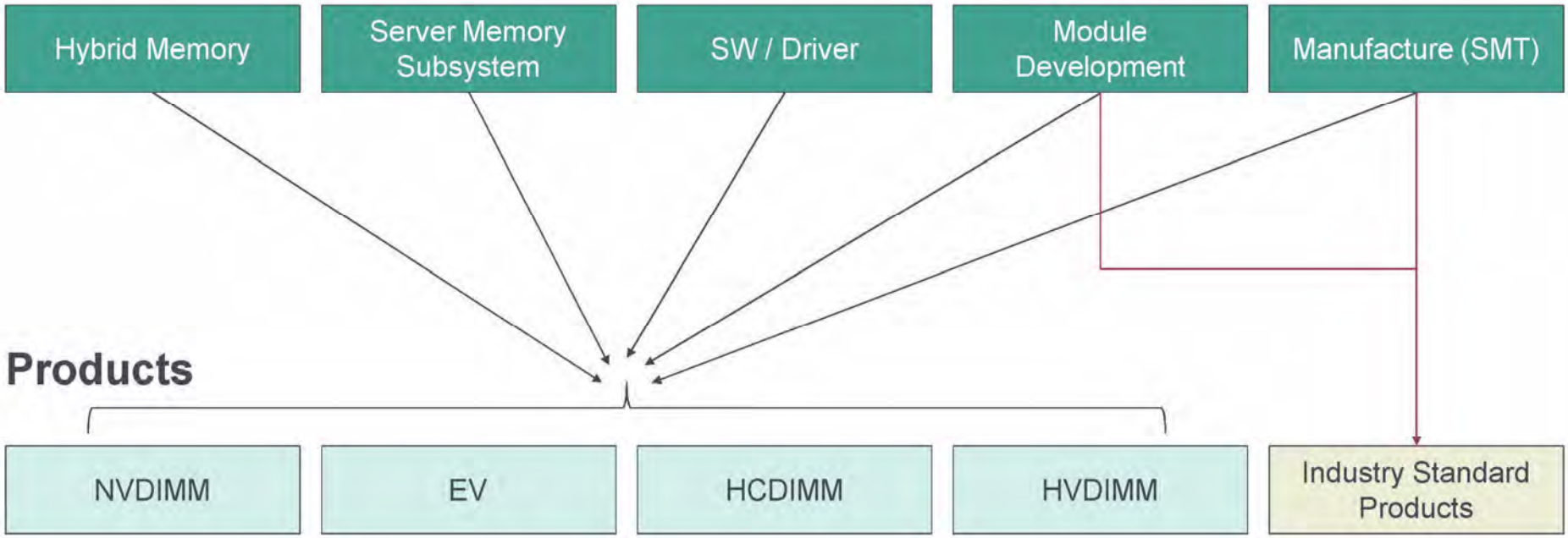
Engineering Capabilities



Netlist Key Technologies and Products

Technologies



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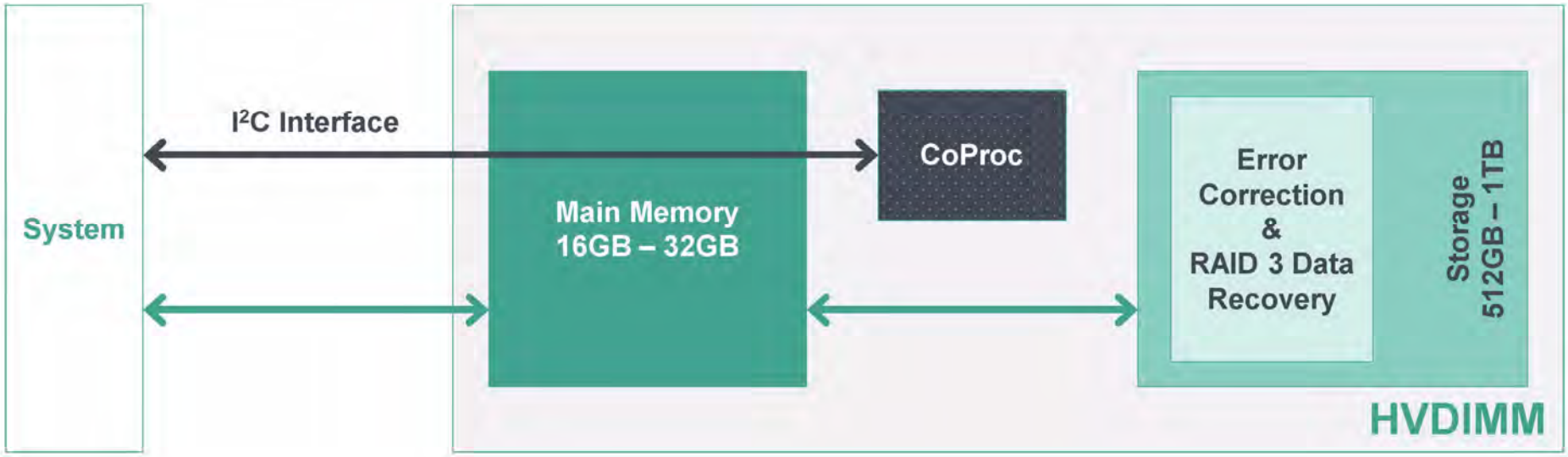
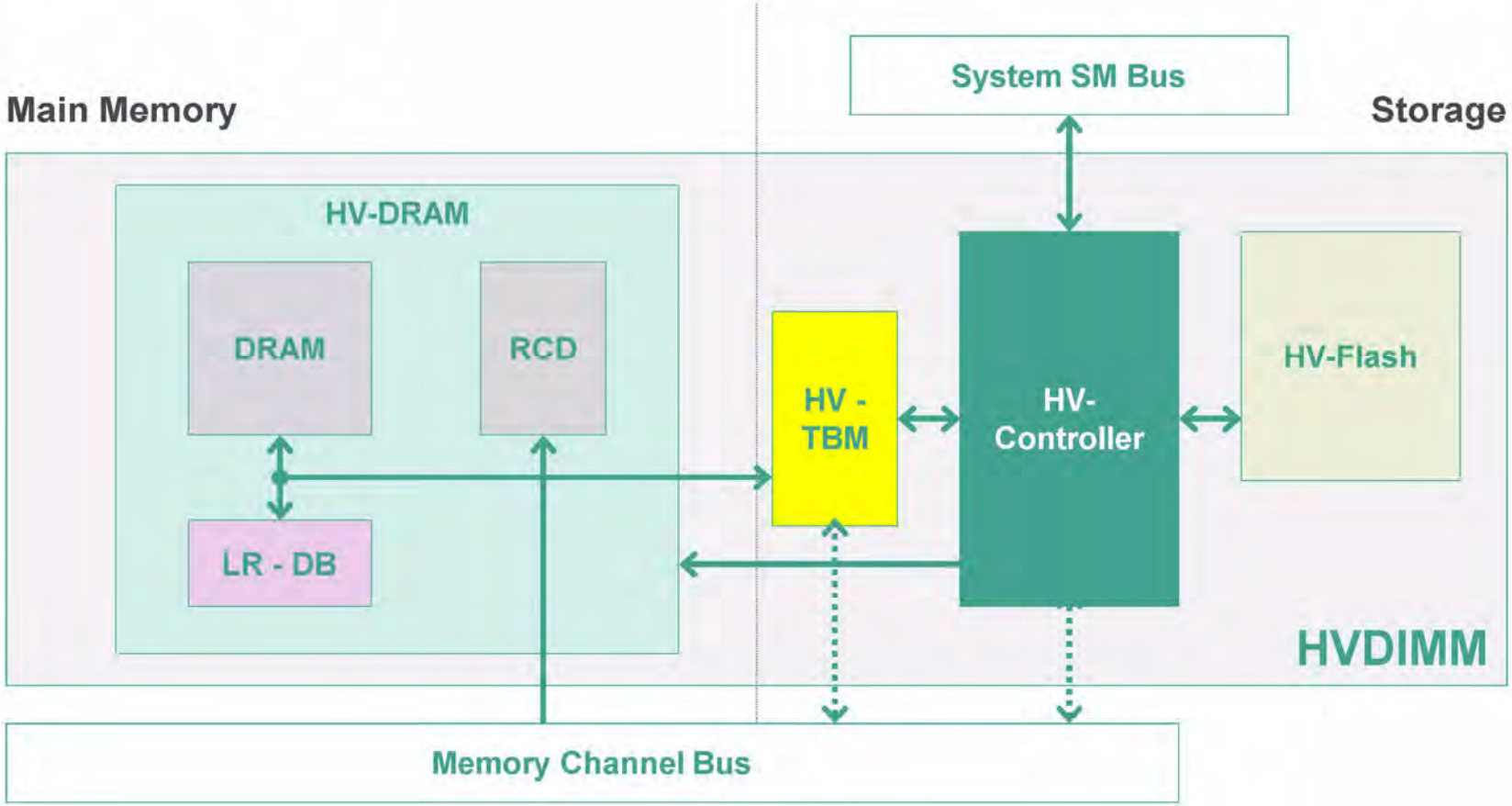
What is HVDIMM

- On-module coprocessor performs dynamic error-correction, data recovery and data reconstruction – RAID 3 storage
- Data transfer to/from System via the memory channel
- All asynchronous communication via I2C bus – ex. Performance monitor



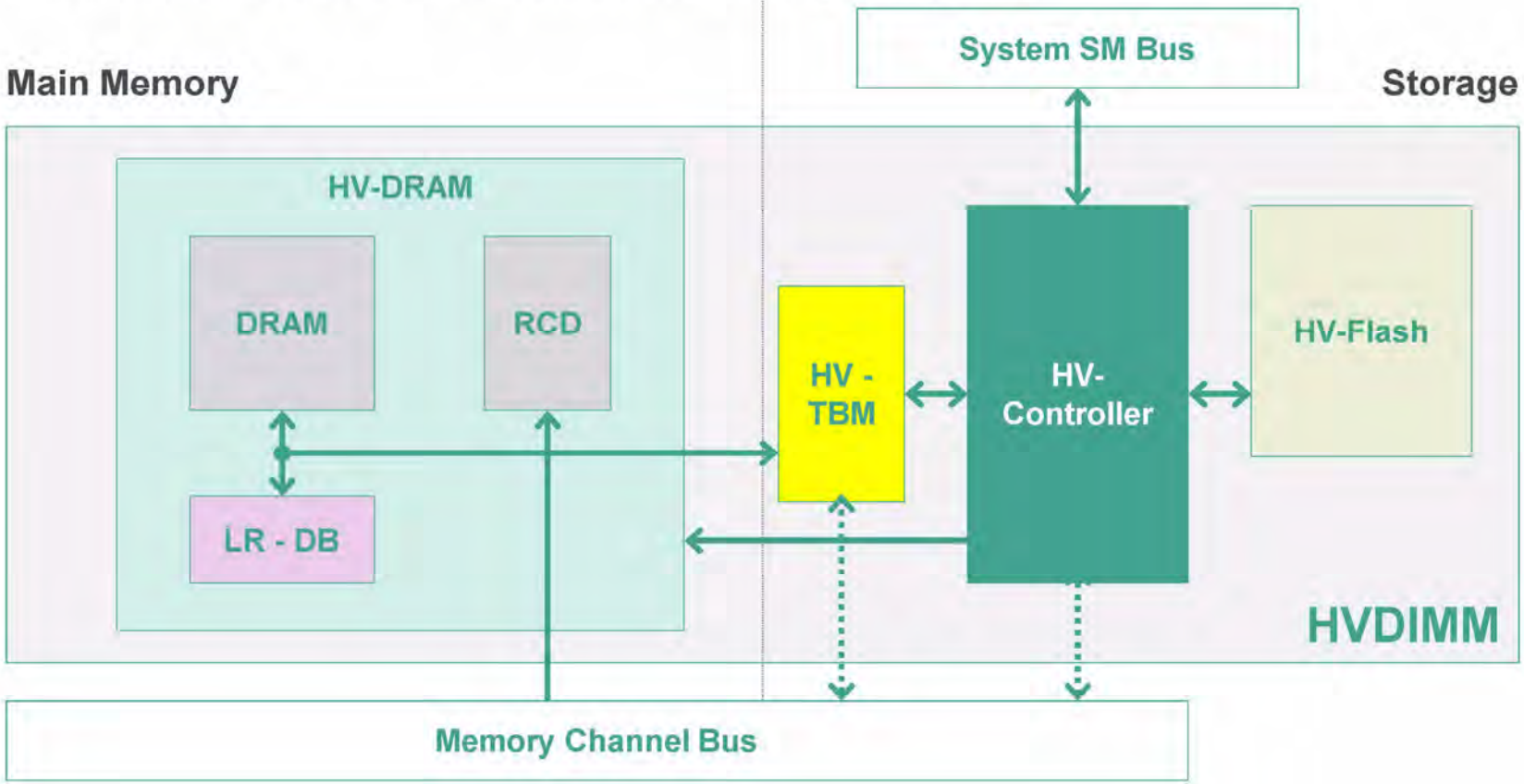
HyperVault Technology

- **TBM (Temporary Buffer Memory)**
  - Minimizes HV-Flash write (all intermediate writes to HV-TBM)
  - Serves as Data Cache to HV-DRAM (Main Memory)
  - Serves as Flow Rate Control Buffer



HyperVault Technology

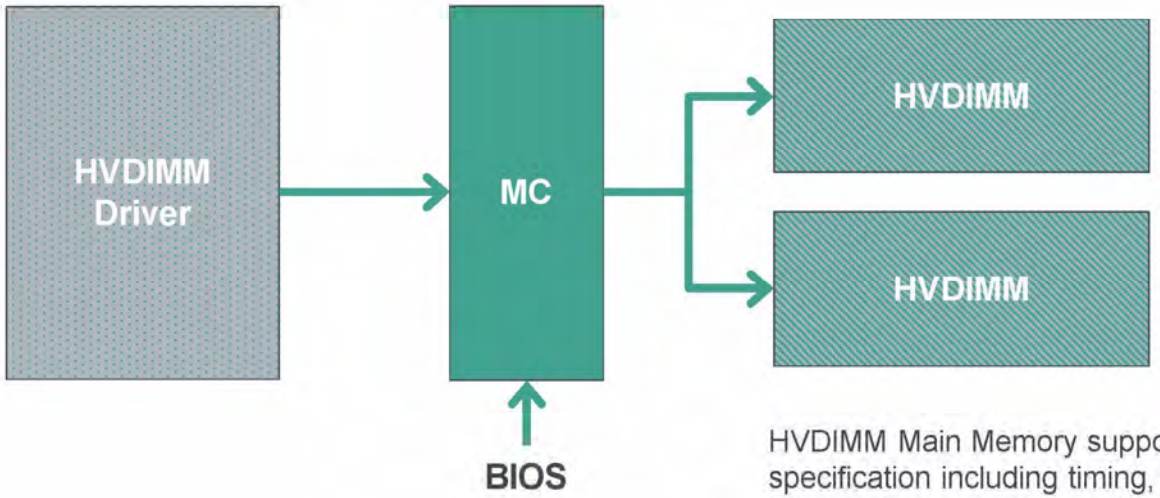
- **Persistent Main Memory**
  - NV operation on HV-TBM, and HV-DRAM
- **RDMA (Remote DMA) operation via MMIO between HV-TBM and HV-Flash**
  - Data transfer between HV-TBM and HV-Flash in background operation



Netlist Interceptor System Software

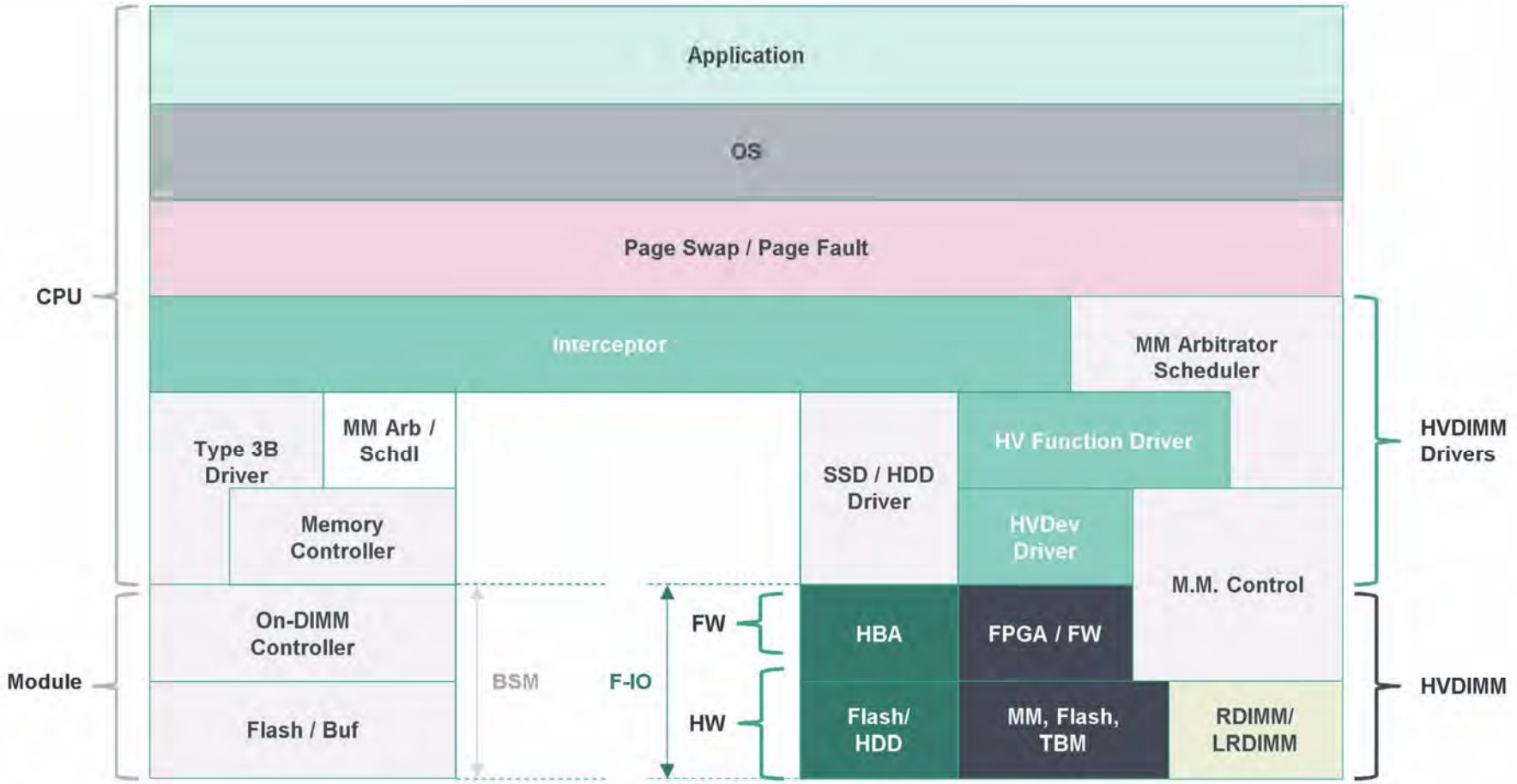
No BIOS Modification Required

- HVDIMM Driver send memory Read/Write access requests to Memory Controller (MC). All Memory (DRAM and Flash) access to/from HVDIMM is fully controlled by MC (by executing the memory access request from HVDIMM Driver).
- HVDIMM Controller monitors and address and control signal from MC to dynamically support different operations.
- HVDIMM Driver modifies the E820 system address space based on the HVDIMM SPD to be able to control the data transfer between the system address space and the HVDIMM address space.



HVDIMM Main Memory supports full LRDIMM specification including timing, read/write address interleaving, rank/channel interleaving, and CAS read/write latency.

HyperVault Software Hierarchy

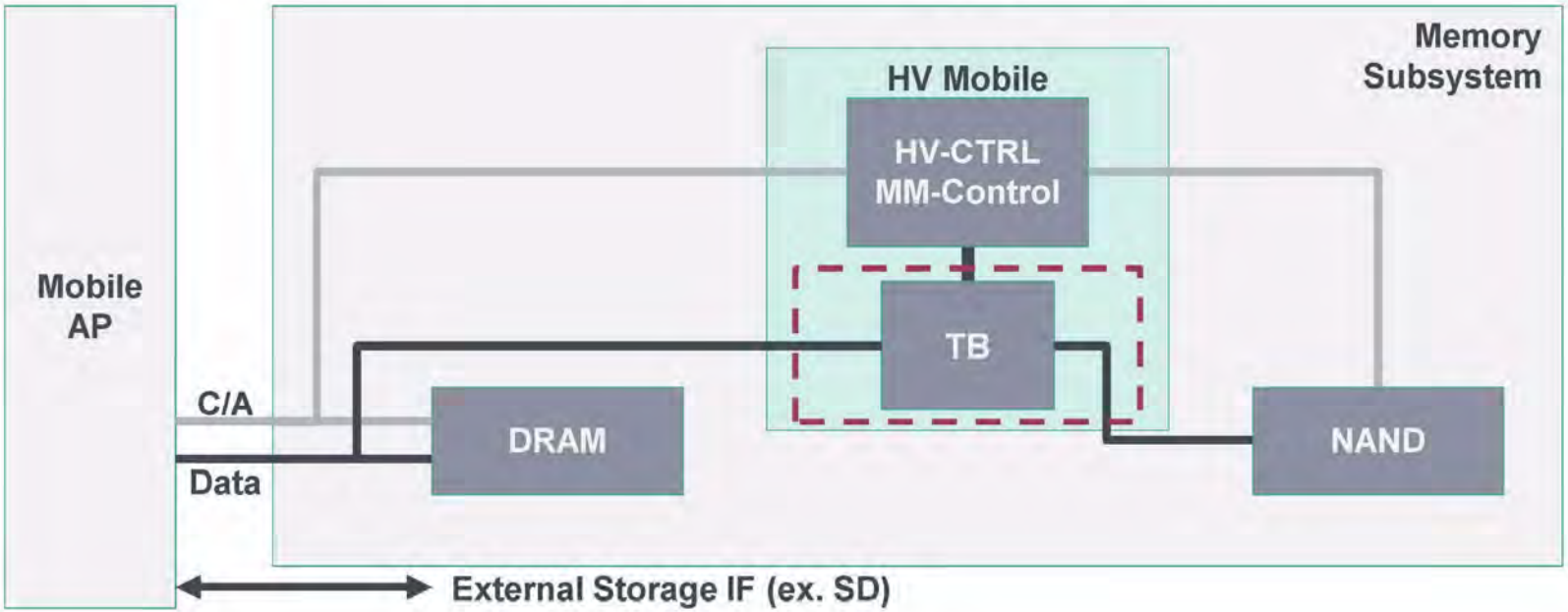


Netlist HV-DIMM Technical Capabilities

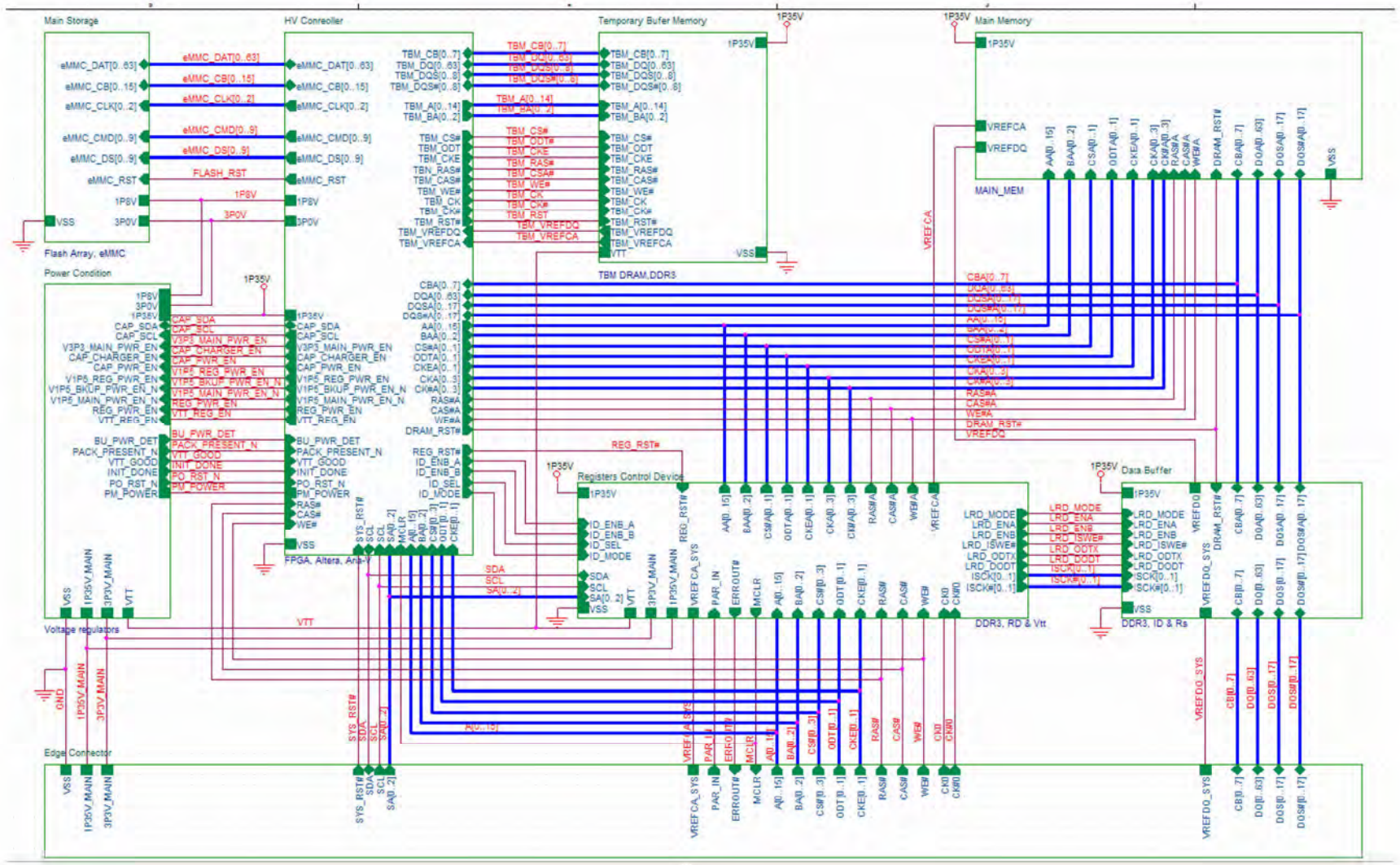
Storage system I/F	Supplier to a number of storage manufactures
Memory Sub system Design	Proven history with HCDIMM (No BIOS changes) and NVDIMM
Patent development	Multiple Memory subsystem patent
ASIC development	Work with ASIC design house
IO – Phy development	
Component testing in system	Extensive experience in FAE analysis on passive and active components, AMB, Registers, DRAM, and DIMM behavior in the system environment
System bring up	Proven history with HC-DIMM (non JEDEC DIMM with JEDEC interface) and NV-DIMM
Software/Firmware	SW engineers with driver and firmware experiences
Co-processor IP	Some experiences with FPGA embed processor
Product manufacture	SZ factory

HV-MCP Mobile

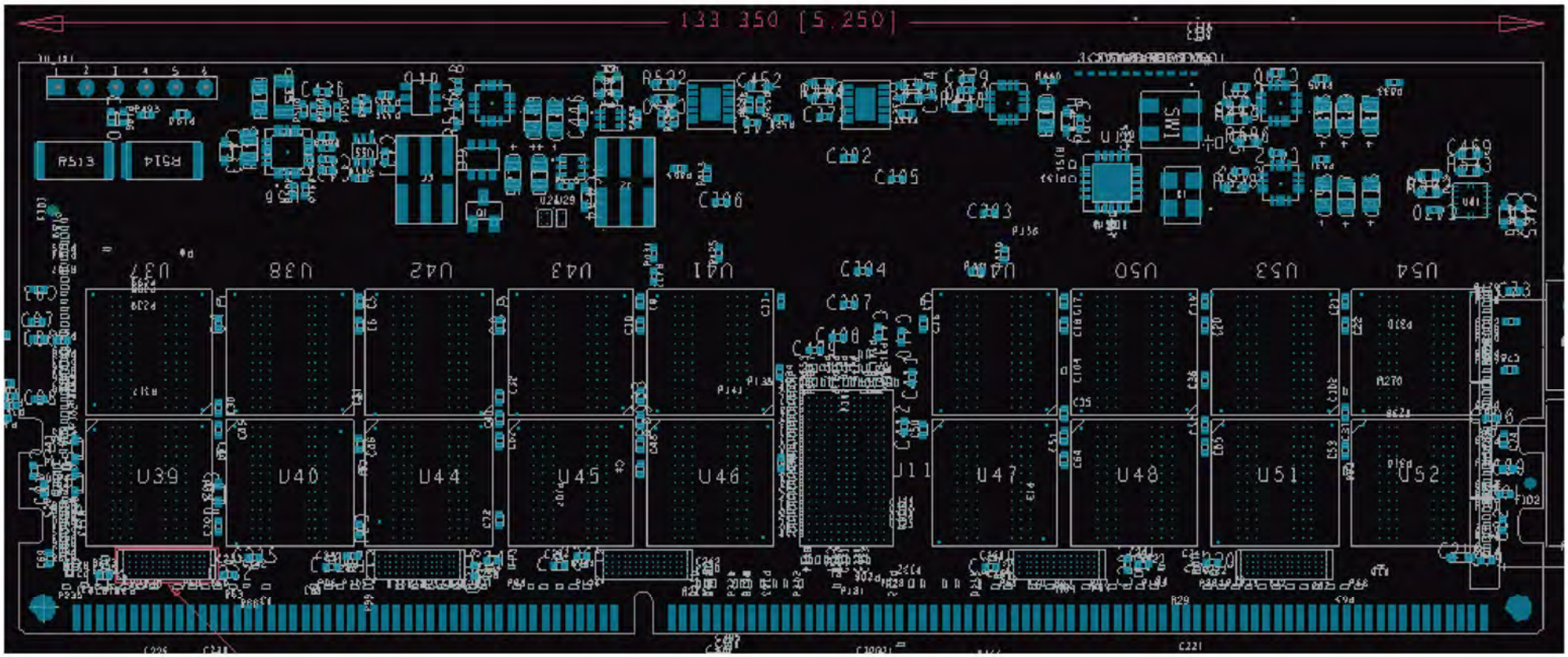
- **Mobile Memory Subsystem**
  - High-end memory system with low density DRAM
  - Cost and power reduction technology
  - Direct DRAM-Flash (Device-Storage) interface
  - Eliminates AP-Flash (Device-Storage) interface



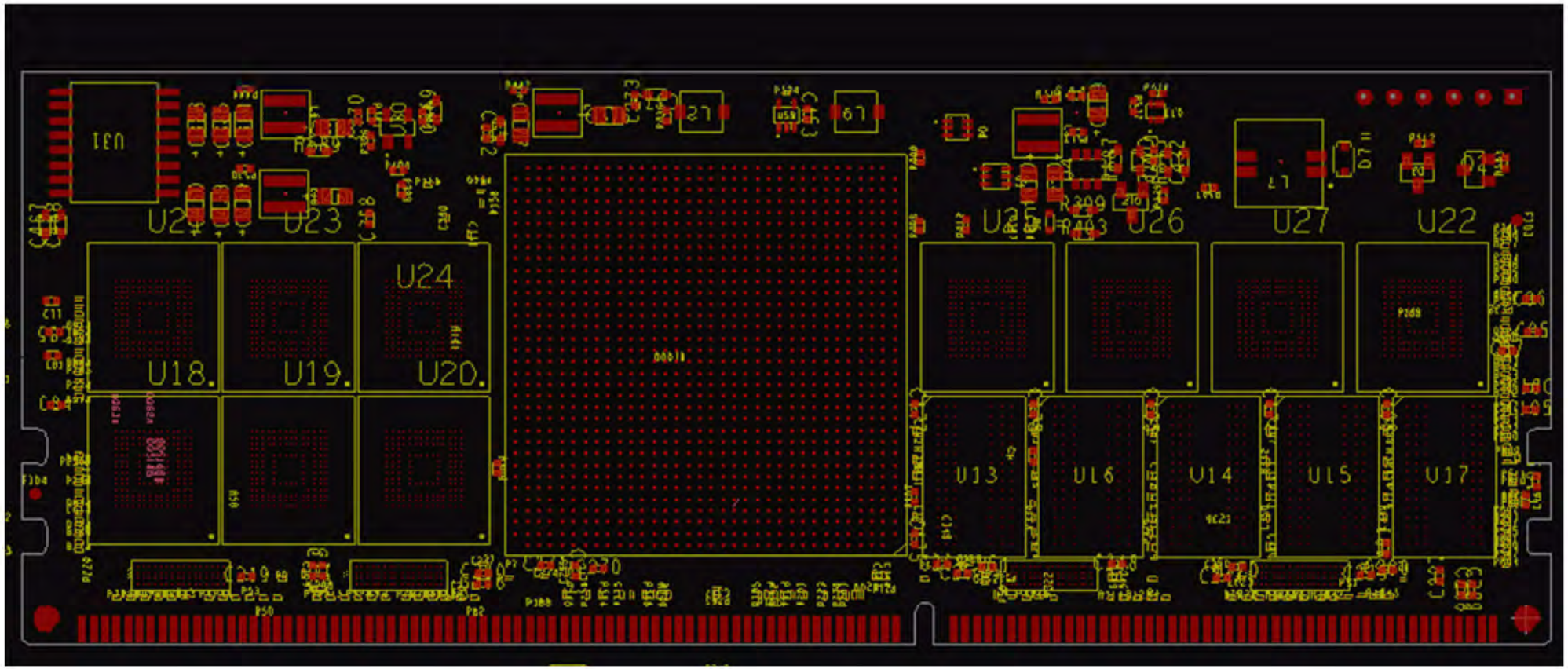
HVDIMM POC Detail Block Diagram



HVDIMM POC PCB Placement (Top Side)



HVDIMM POC PCB Placement (Bottom Side)



HVDIMM POC Project Schedule

HVDIMM PCB design Schedule	106 days	2/2/2015	6/29/2015
Schematic design and entry in Orcad CSI by Cadence	89 days	2/2/2015 8:00	6/4/2015 17:00
Part list and Netlist creation	5 days	2/2/2015 8:00	2/6/2015 17:00
Part placement on PCB (Allegro PCB designer by Cadence	22 days	3/16/2015 8:00	4/14/2015 17:00
Pre route simulation and constraint creation	5 days	4/15/2015 8:00	4/21/2015 17:00
Routing of all signals on PC	10 days	4/22/2015 8:00	5/5/2015 17:00
Post route simulation	5 days	5/6/2015 8:00	5/12/2015 17:00
PCB design review for fab.	1 day	5/13/2015 8:00	5/13/2015 17:00
Gerber file generation	1 day	5/13/2015 8:00	5/13/2015 17:00
PCB fab (in China)	15 days	5/14/2015 8:00	6/3/2015 17:00
PCB receive (in China)	1 day	6/4/2015 8:00	6/4/2015 17:00
Module assembly	17 days	6/5/2015 8:00	6/29/2015 17:00
2 Module without FPG	2 days	6/5/2015 8:00	6/8/2015 17:00
5 with FPG	2 days	6/5/2015 8:00	6/8/2015 17:00
Ship to Irvine	5 days	6/9/2015 8:00	6/15/2015 17:00
First power up HVDIMM as RDIMM (DRAM only)	5 days	6/16/2015 8:00	6/22/2015 17:00
Load FPGA code and test other HVDIMM functions	5 days	6/23/2015 8:00	6/29/2015 17:00

NVDIMM Roadmap

Density	Voltage (V)	Speed	2014		2015				2016				2017	
			Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
DDR3 NVvault®														
4GB SLC	1.35 / 1.5	1600	MP											
8GB MLC	1.35 / 1.5	1600	MP											
16GB MLC	1.35	1333		TBD	ES	CS	MP							
DDR4 NVault®														
8GB MLC RDIMM	1.2	2133					ES	CS	MP					
16GB MLC RDIMM	1.2	2133					ES	CS	MP					
16GB MLC LRDIMM	1.2	2667							ES	CS	MP			
32GB MLC LRDIMM	1.2	2667							ES	CS	MP			
DDR4 HVault®														
16GB 512GB MLC	1.2	3200					POC	ES	CS	MP				
32GB 1TB MLC	1.2	3200						ES	CS	MP				

HV Server – Engineering Budget

YR	2014						2015								2016								2017			
QTR	Q2		Q3		Q4		Q1		Q2		Q3		Q4		Q1		Q2		Q3		Q4		Q1		Q2	
Type	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H	S	H
Staff	2	2	2	3	3	5	3	5	4	5	4	5	3	4	2	1	1	1	1	0	1	0	1	0	1	0
Server ($K)	164		266		410		400		450		450		350		150		100		50		50		50		50	
Total ($M) per Year	1.0						1.65								.350								.100			

Not included: ASIC and Tool Cost: $5.0M

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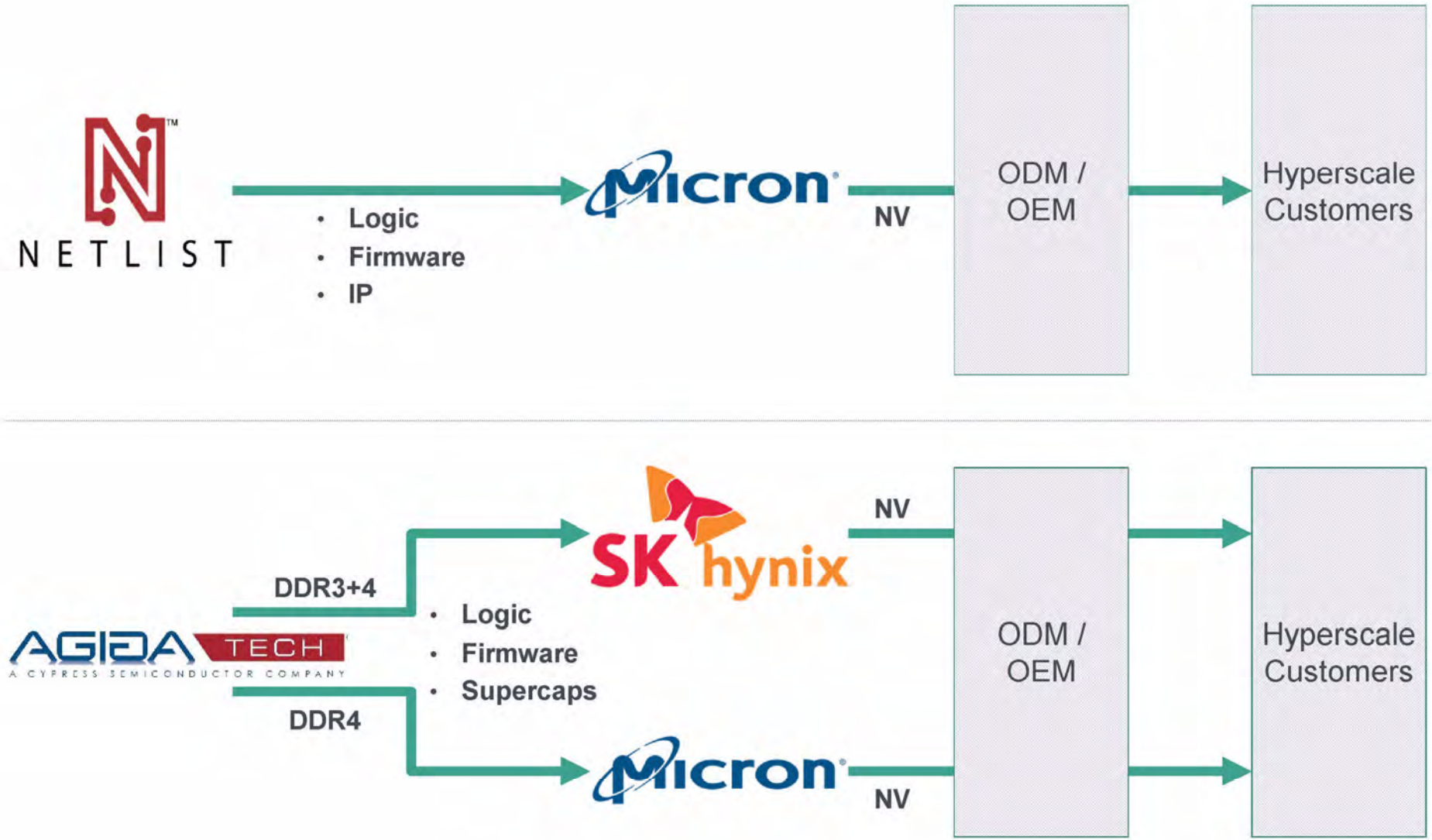
NVDIMM Partnership Model

Joint Development



Proposed Strategic Partnership

Joint Development (excluding mobile and LRDIMM)

	Netlist	Micron	
Technology investment in HV and NV	✓		
NRE for HV development			
+ exclusivity		✓	**Period TBD**
Development Costs:			
• Chipset	✓✓		
• Module	✓	✓	
• Software/Firmware	✓	✓	
Equity Investment:			
• Convertible debt		✓	
Sales:			
• Chipsets	✓✓		
• Modules	✓	✓	
Royalty payable on			
• sales of HV Modules	✓	✓	
• sales of NV Modules	✓	✓	

Proposed Strategic Partnership

Technology and IP Collaboration

	Netlist	Micron	
Technology Collaboration			
• HyperVault	✓		
• NVDIMM	✓		
Intellectual Property			
• All Netlist Patents			
• *LRDIMM*	✓		
• *Hybrid Memory*	✓		
Payments			
• *Option A*		✓	$$ Upfront/ongoing: 10-year term
• *Option B*		✓	$ Upfront/ongoing: 5-year term
Investment			
• *Convertible Debt*		✓	
Cross Covenant Not to Sue	✓	✓	

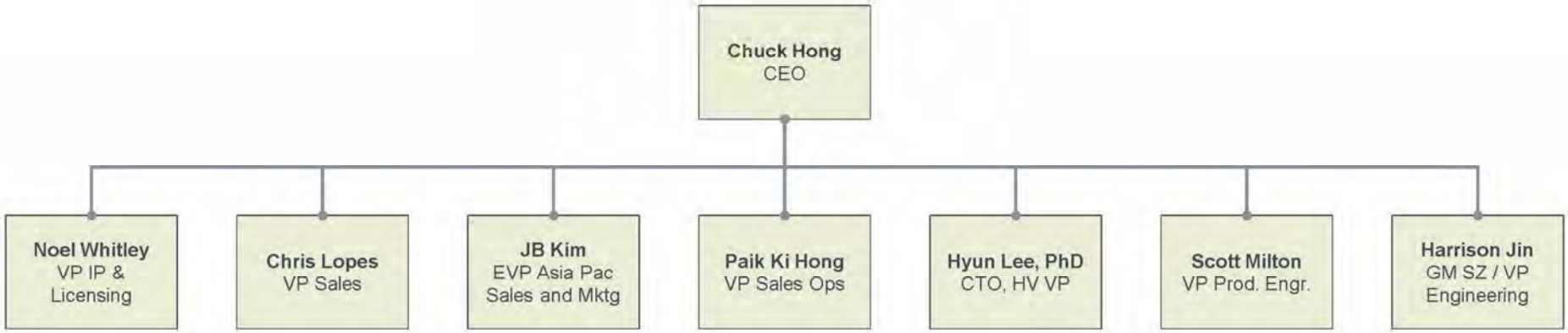
Proposed Strategic Partnership

Technology and IP Collaboration

	Netlist	Partner	
Technology Collaboration			
- HyperVault	✓		
- NVDIMM	✓		
Intellectual Property			
- All Netlist Patents			
- *LRDIMM*	✓		
- *Hybrid memory*	✓		
Payments			
- *Option A*		✓	$$ Upfront/ongoing -- 10 year term
- *Option B*		✓	$ Upfront/ongoing -- 5 year term
Investment			
- *Convertible Debt*		✓	
Cross Covenant Not to Sue	✓	✓	

Appendix

Management Organization



Example Hybrid Claim Analysis: 8,301,833